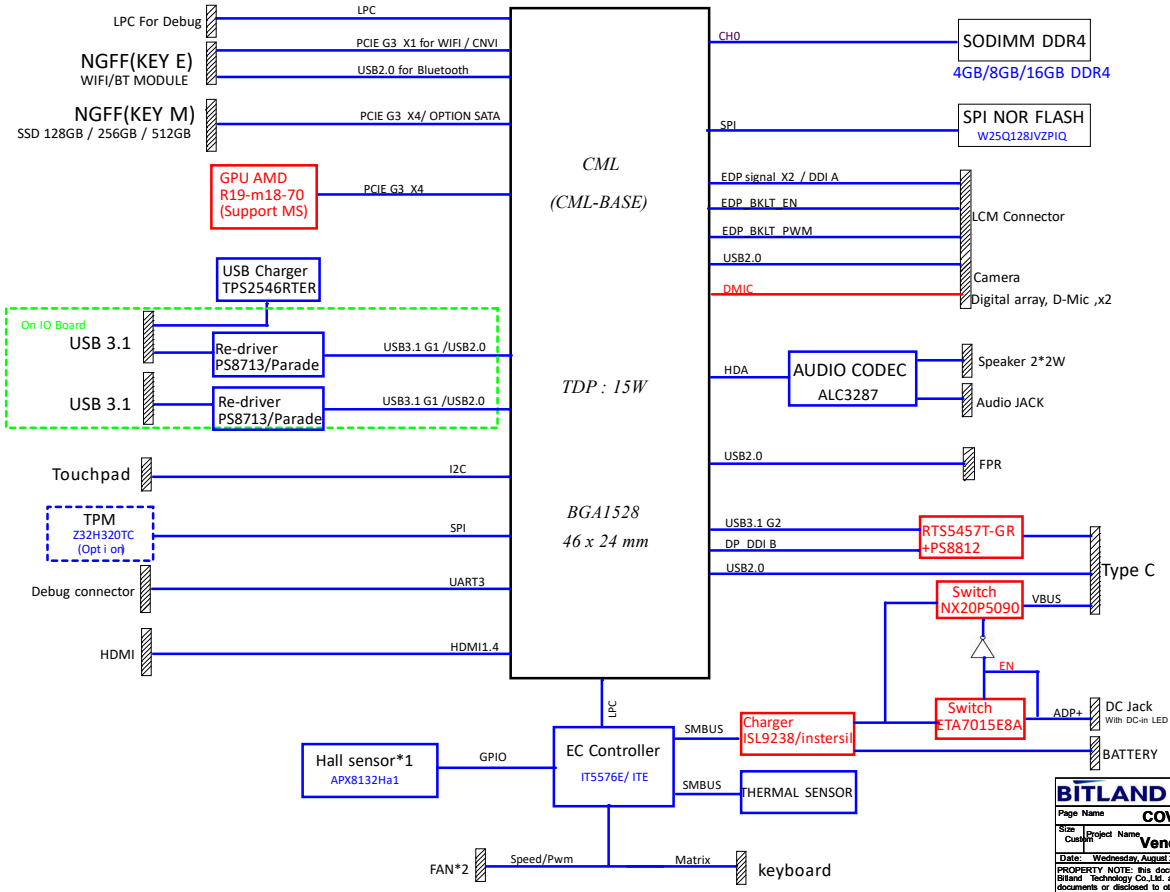
Veneno for Lenovo



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06--CML-U(4/12)HDA,EMMC,SD
07--CML-U(5/12)CLK,GPIO
08--CML-U(6/12)GPIO
09--CML-U(7/12)PCIE,USB,SATA
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18--NA
19--SODIMM_CHB
20--Sequence&Power Map
21--NA
22--NA
23--NA
24--SYSTEM FLASH
25--NA
26--PCIE SSD MODULE
27--NA
28--FP
29--CPU THERMAL SENSOR
30--FAN conn
31 -- NA
32 -- HDMI CONN
33 -- NA
34 -- NA
35 -- TPM2.0
36 -- DISPLAY
37 -- NA
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62--NA
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64--PWR-Load Switch
65--PWR-+1.8V_PRIM
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73--POWER MAP
74--GPU PCIE
75--GPU MEN
76--GPU GPIO MISC
77--GPU DP INTERFACE
78--NA
79--GPU POWER&GND
80--GPU_RAM(GDDR5)
81--GPU MS
82--NA
83--IO Board_IO CONNECTOR
84--IO Board_USB3.0 Redriver
85--IO Board_USB3.0_AOU
86--IO Board_USB3.0_PORT2
87--IO Board_SWITCH & LED

INTERNAL ONLY

BPAGE DRAWING

#by_jy_#rd_
Wed Jun 03 11:22:42 2015

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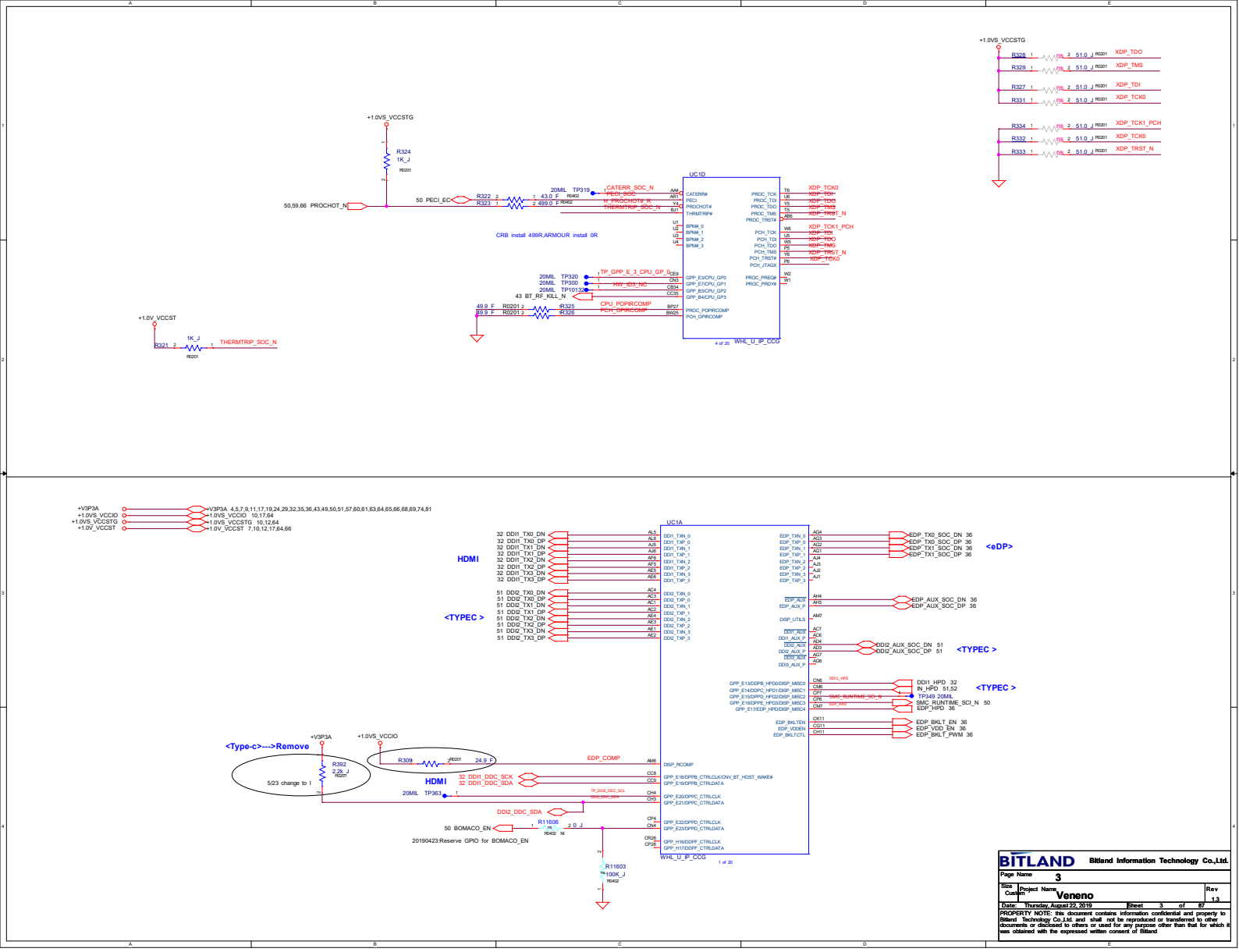

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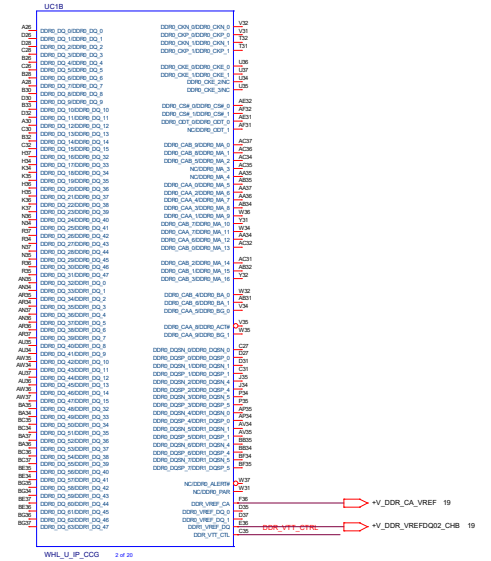

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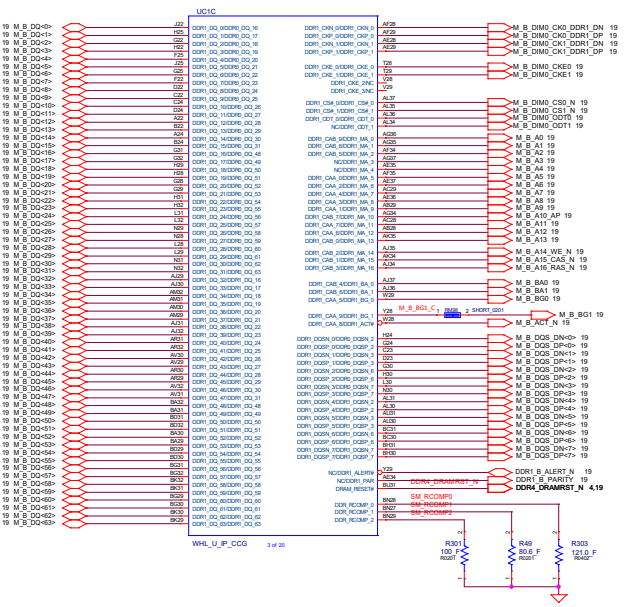

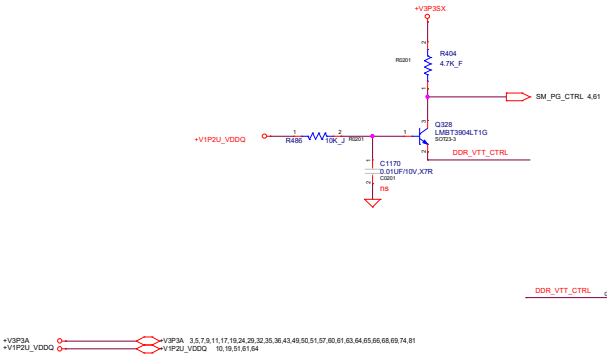

Default

Memory size	4Gb or 8Gb	16Gb
DRAM M9 pin	RM95,RM96,RM97,RM98 need uninstall RM99,RM100 need install	RM95,RM96,RM97,RM98 need install RM99,RM100 need uninstall
DRAM E9 pin	RM79,RM81,RM83,RM85, RM87,RM89,RM91,RM93 need install 0 ohm	RM79,RM81,RM83,RM85, RM87,RM89,RM91,RM93 need install 240 ohm
SOC RCOMP0	RM3 200 ohm need install	RM3 121 ohm need install

page4, 19,20

page19,20

page4

2/2 Add (4Gb 8Gb) & (16Gb) BOM option table

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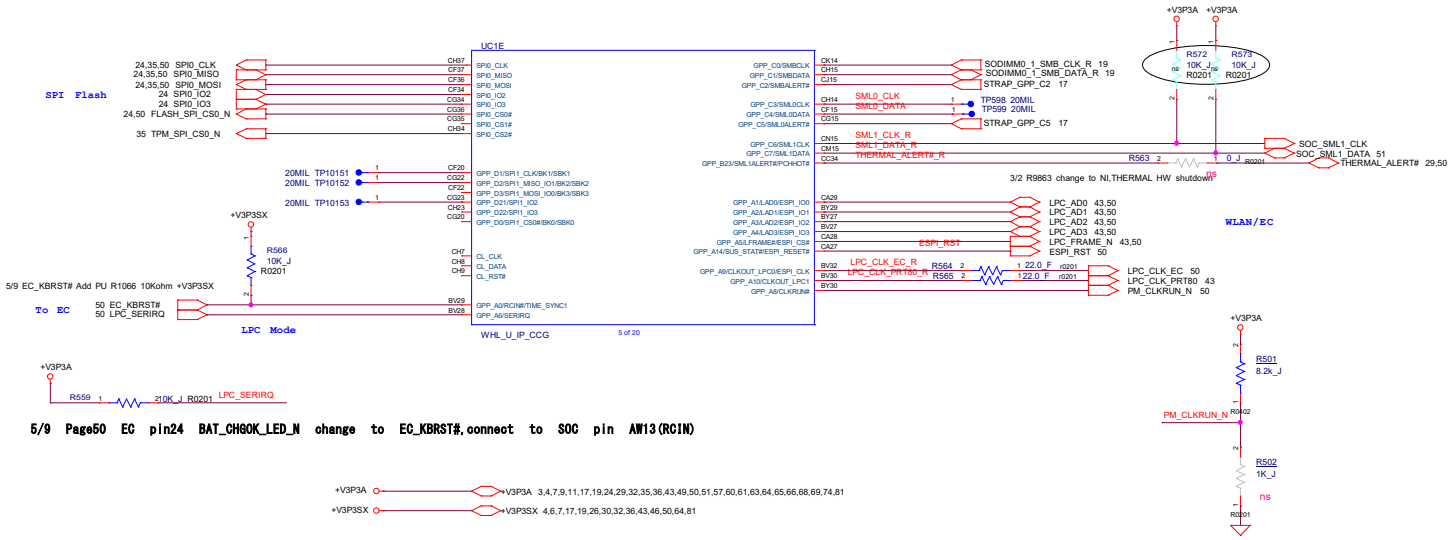

5/9 Page50 EC pin24 BAT_CHGOK_LED_N change to EC_KBRST#,connect to SOC pin AW13(RCIN)

+V3P3A → +V3P3A 3,4,7,9,11,17,19,24,29,32,35,36,43,49,50,51,57,60,61,63,64,65,66,68,69,74,81

+V3P3SX → +V3P3SX 4,6,7,17,19,26,30,32,36,43,46,50,64,81

SPI0_MOSI	Reserved	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_MISO	Reserved	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_IO2	Reserved	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_IO3	Reserved	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

SMBALERT# / GPP_C2	TLS Confidentiality	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **Disable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1 = **Enable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
SML0ALERT# / GPP_C5	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **LPC** Is selected for EC. (Default) 1 = **eSPI** Is selected for EC. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
SML1ALERT# / PCHHOT# / GPP_B23	Reserved	Rising edge of RSMRST#	This signal has an internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.

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To Enable ME Override

ME_Flash_EN — R648 1K_J — R0402 — STRAP_HDA_SDO_SOC

Difference with armour
Add EC to enable ME override

5/23 R9848 install,BIOS request

HDA_SDO/ I2S_TXD0	Flash Descriptor Security Override	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = **Enable** security measures defined in the Flash Descriptor. (Default) 1 = **Disable** Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. ***Notes:*** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. Asserting HDA_SDO high on the rising edge of PCH_PWROK will also halt Intel Management Engine after Chipset bring up and disable runtime Intel ME features. This is a debug mode and must not be asserted after manufacturing/debug. 3. This signal is in the primary well.
SPKR / GPP_B14	Top Swap Override	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "Top Swap" mode. (Default) 1 = **Enable** "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64-KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap . ***Notes:*** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. Software will not be able to clear the Top Swap bit until the system is rebooted. 3. The status of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DCh, bit4). 4. This signal is in the primary well.

46 HDA_SYNC — R693 22.0_F 0201 — HDA_SYNC_SOC
46 HDA_BCLK_R — R686 33.0_J R0201 — HDA_BCLK
46 STRAP_HDA_SDO — R695 22.0_F 0201 — STRAP_HDA_SDO_SOC
HDA_RST_N_SOC

Rev_0.53

HDA for AUDIO

UC1G

HDA_SYNC_SOC
HDA_BCLK
STRAP_HDA_SDO_SOC
HDA_SDI0
46 HDA_SDI0
20MIL TP10138 — HDA_RST_N_SOC

BN24 HDA_SYNC/I2S0_SFRM
BN27 HDA_BCLK/I2S0_SCLK
BN26 HDA_SDO/I2S0_TXD
BN25 HDA_SDI0/I2S0_RXD
BL36 HDA_SDI1/I2S1_RXD/SNDW1_DATA
BL35 HDA_RST#/I2S1_SCLK/SNDW1_CLK
CK23 GPP_D23/I2S_MCLK
BL37
BL34 I2S1_SFRM/SNDW2_CLK
I2S1_TXD/SNDW2_DATA

CH36 GPP_G0/SD_CMD
CL35 GPP_G1/SD_DATA0
CL36 GPP_G2/SD_DATA1
CM35 GPP_G3/SD_DATA2
CN35 GPP_G4/SD_DATA3
CH35 GPP_G5/SD_CD#
CK36 GPP_G6/SD_CLK
CK34 GPP_G7/SD_WP — TP_SD_WP — R664 ns 0_J R0201

20180430
43 CNVI_RF_RESET_N — 20MIL TP10125
43 XTAL_CLKREQ — 20MIL TP10126
20MIL TP10161 — WIFI_DISABLE_N_R

CJ32 GPP_H1/I2S2_SFRM/CNV_BT_I2S_BCLK/CNV_RF_RESET#
CH32 GPP_H0/I2S2_SCLK/CNV_BT_I2S_SCLK
CH29 GPP_H2/I2S2_TXD/CNV_BT_I2S_SDI/MODEM_CLKREQ
CH30 GPP_H3/I2S2_RXD/CNV_BT_I2S_SDO
CP24 GPP_D19/DMIC_CLK0/SNDW4_CLK
CN24 GPP_D20/DMIC_DATA0/SNDW4_DATA

BW36 GPP_A17/SD_VDD1_PWR_EN#/ISH_GP7
BY31 GPP_A16/SD_1P8_SEL
CK33 SD_1P8_RCOMP
CM34 SD_3P3_RCOMP

43 WIFI_DISABLE_N — R11614 SHORT_0201 — WIFI_DISABLE_N_R
36,46 DMIC_CLK — R11533 SHORT_0402 — DMIC_CLK_CPU
36,46 DMIC_DATA — R11534 SHORT_0402 — DMIC_DATA_CPU
17,46,50 HDA_SPKR

WLAN_DET_N 43,81
R11478 ns 200_J R0201
R615 200_J R0201

CK25 GPP_D17/DMIC_CLK1/SNDW3_CLK
CJ25 GPP_D18/DMIC_DATA1/SNDW3_DATA
CF35 GPP_B14/SPKR

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Difference with armour
Add 0ohm NI

1/4 Connect codec

+V3P3A
+V3P3SX

+V3P3A 3,4,5,7,9,11,17,19,24,29,32,35,36,43,49,50,51,57,60,61,63,64,65,66,68,69,74,81
+V3P3SX 4,5,7,17,19,26,30,32,36,43,46,50,64,81

UC1I

43 CNVI_WGR_DATA0_DN — CR30 CNV_WR_D0N
43 CNVI_WGR_DATA0_DP — CP30 CNV_WR_D0P
43 CNVI_WGR_DATA1_DN — CM30 CNV_WR_D1N
43 CNVI_WGR_DATA1_DP — CN30 CNV_WR_D1P
43 CNVI_WT_DATA0_DN — CN32 CNV_WT_D0N
43 CNVI_WT_DATA0_DP — CM32 CNV_WT_D0P
43 CNVI_WT_DATA1_DN — CP33 CNV_WT_D1N
43 CNVI_WGR_CLK_DN — CN31 CNV_WR_CLKN
43 CNVI_WGR_CLK_DP — CP31 CNV_WR_CLKP
43 CNVI_WT_CLK_DN — CP34 CNV_WT_CLKN
43 CNVI_WT_CLK_DP — CN34 CNV_WT_CLKP
CNV_WT_RCOMP — CP32 CNV_WT_RCOMP_1
CR32 CNV_WT_RCOMP_2

CN27 GPP_H18/CPU_C10_GATE# — GPPC_H18_BOOTMPC — GPPC_H18_BOOTMPC 64
CM27 GPP_H19/TIMESYNC_0 — R11549 ns 0_J R0201 — BOMACO_EN 39
CF25 GPP_H21 — GPP_H21 — GPP_H21 17
CN26 GPP_H22
CM26 GPP_H23 — TP662 20MIL
CK17 GPP_F10

20190219: add 'BOMACO_EN' for dGPU MS design
3/27 Add TP662

BV35 GPD7 — GPD_7
CN20 GPP_F3 — GPD_7 17

CG25 GPP_D4/IMGCLKOUT0/BK4/SBK4 — CSI2_FLASH_STROBE — TP661 20MIL
CH25 GPP_H20/IMGCLKOUT1

3/18 Add TP661

CR20 GPP_F12/EMMC_DATA0
CM20 GPP_F13/EMMC_DATA1
CN19 GPP_F14/EMMC_DATA2
CM19 GPP_F15/EMMC_DATA3
CN18 GPP_F16/EMMC_DATA4
CR18 GPP_F17/EMMC_DATA5
CP18 GPP_F18/EMMC_DATA6
CM18 GPP_F19/EMMC_DATA7
CM16 GPP_F20/EMMC_RCLK
CP16 GPP_F21/EMMC_CLK
CR16 GPP_F11/EMMC_CMD
CN16 GPP_F22/EMMC_RESET#
EMMC_RCOMP
CK15 EMMC_RCOMP — R614 200_J R0201

+V3P3SX
R673 10K_J R0201
R697 0201 150.0_F
20180430
69,81 PX_EN
R672 10K_J R0201 ns

43 WLAN_COEX3_WWAN — GP20 GPP_F0/CNV_PA_BLANKING
CK19 GPP_F1
CG17 GPP_F2

74 DGPU_HOLD_RST# — CR14 GPP_C8/UART0_RXD
CP14 GPP_C9/UART0_TXD
CN14 GPP_C10/UART0_RTS#
CM14 GPP_C11/UART0_CTS#
GPU_EVENT#_SOC
43 WLAN_COEX1_WWAN — CJ17 GPP_F8/CNV_MFUART2_RXD
43 WLAN_COEX2_WWAN — CH17 GPP_F9/CNV_MFUART2_TXD
CF17 GPP_F23/A4WP_PRESENT

WHL_U_IP_CCG 9 of 20

D6812
LBAT54XV2T1G
sod523
76 GPU_EVENT# — GPU_EVENT#_SOC
ns

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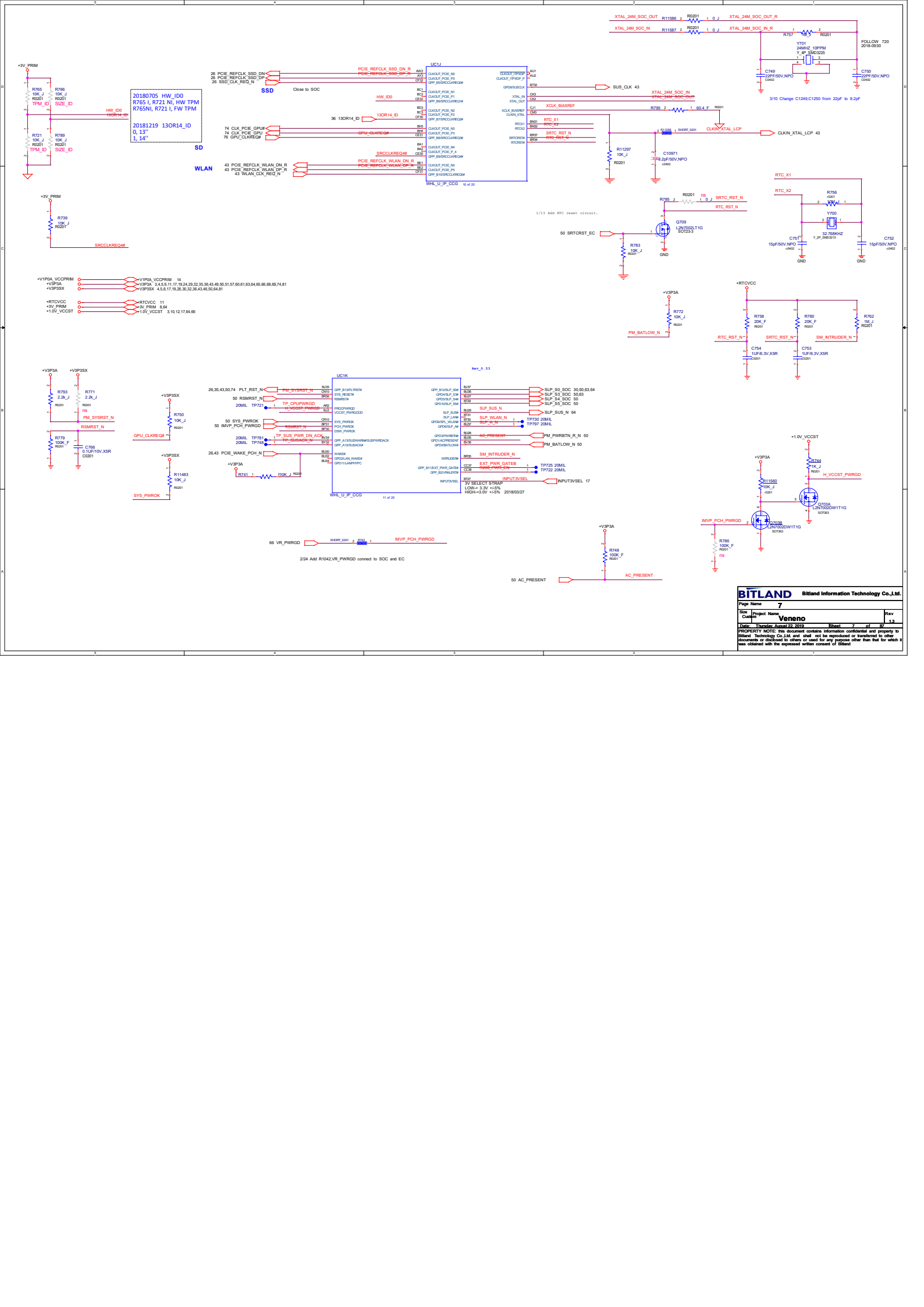
20180705 HW_ID0
R765 I, R721 NI, HW TPM
R765NI, R721 I, FW TPM
20181219 13OR14_ID
0, 13"
1, 14"
SSD
SD
WLAN
Close to SOC
UC1J
UC1K
WHL_U_IP_CCG
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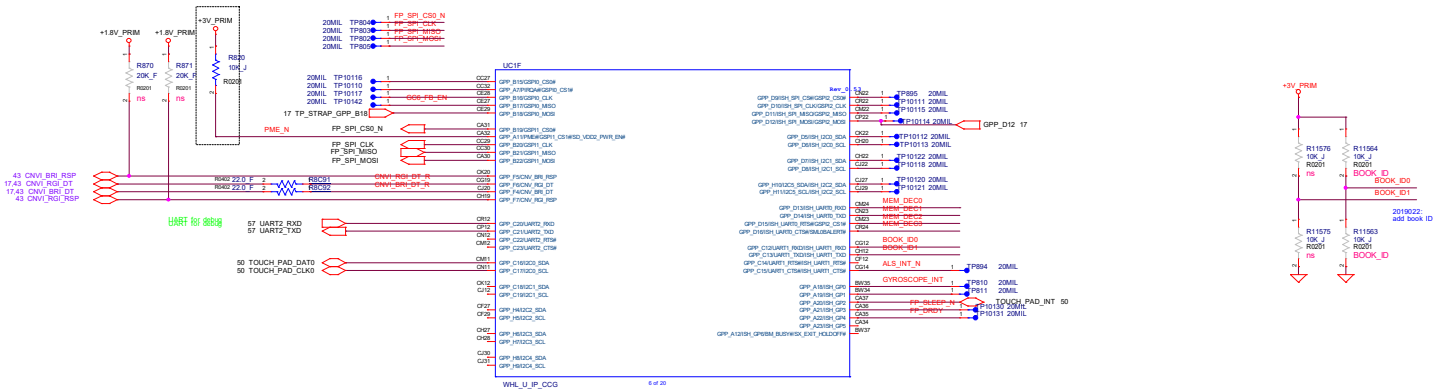
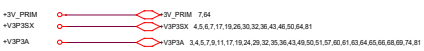
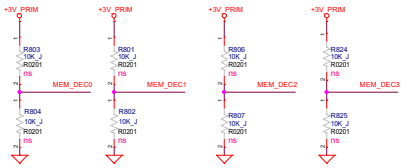




Memory Dectection



SIZE	2GB	4GB	8GB	16GB
MEM_DEC0	0	1	0	1
MEM_DEC1	0	0	1	1

Vender	Samsung	Hynix	Micron	
MEM_DEC2	0	1	0	
MEM_DEC3	0	0	1	

Notes:

1. GPIO F group supports 1.8V only.
2. GPD group supports 3.3V only.

GSPI0_MOSI / GPP_B18	No Reboot	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "No Reboot" mode. (Default) 1 = **Enable** "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP. ***Notes:*** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.

GSPI1_MOSI / GPP_B22	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWROK	This Signal has a weak internal pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function0, offset BCh, bit 6). **Bit 6 — Boot BIOS Destination** 0 — SPI (Default) 1 — LPC ***Notes:*** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination select to LPC by functional strap or using Boot BIOS Destination bit will not affect SPI accesses initiated by Intel ME or Integrated GBE LAN. 4. This signal is in the primary well.

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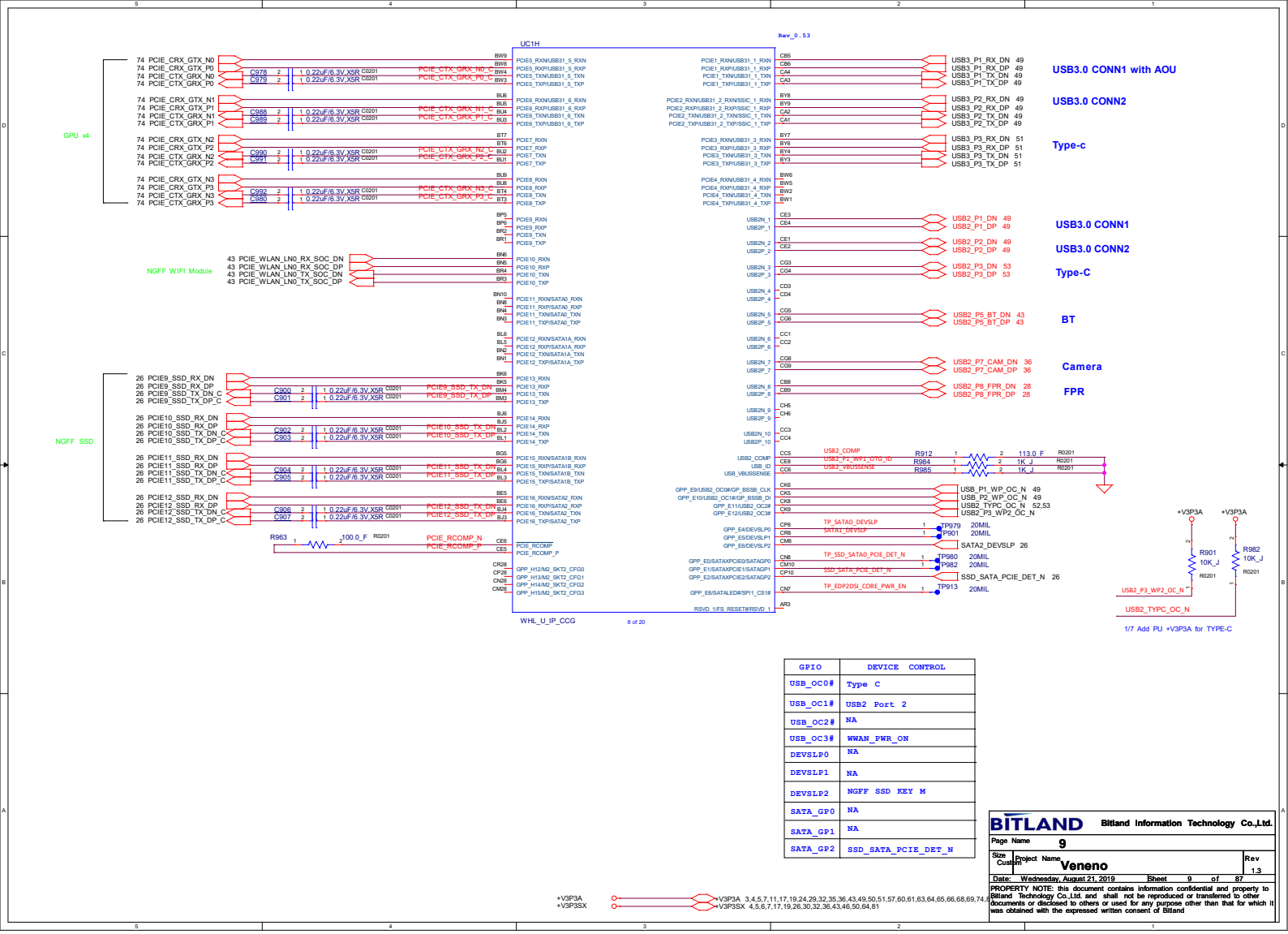

GPIO	DEVICE CONTROL
USB_OC0#	Type C
USB_OC1#	USB2 Port 2
USB_OC2#	NA
USB_OC3#	WWAN_PWR_ON
DEVSLP0	NA
DEVSLP1	NA
DEVSLP2	NGFF SSD KEY M
SATA_GP0	NA
SATA_GP1	NA
SATA_GP2	SSD_SATA_PCIE_DET_N

+V3P3A
+V3P3SX
+V3P3A 3,4,5,7,11,17,19,24,29,32,35,36,43,49,50,51,57,60,61,63,64,65,66,68,69,74,8
+V3P3SX 4,5,6,7,17,19,26,30,32,36,43,46,50,64,81

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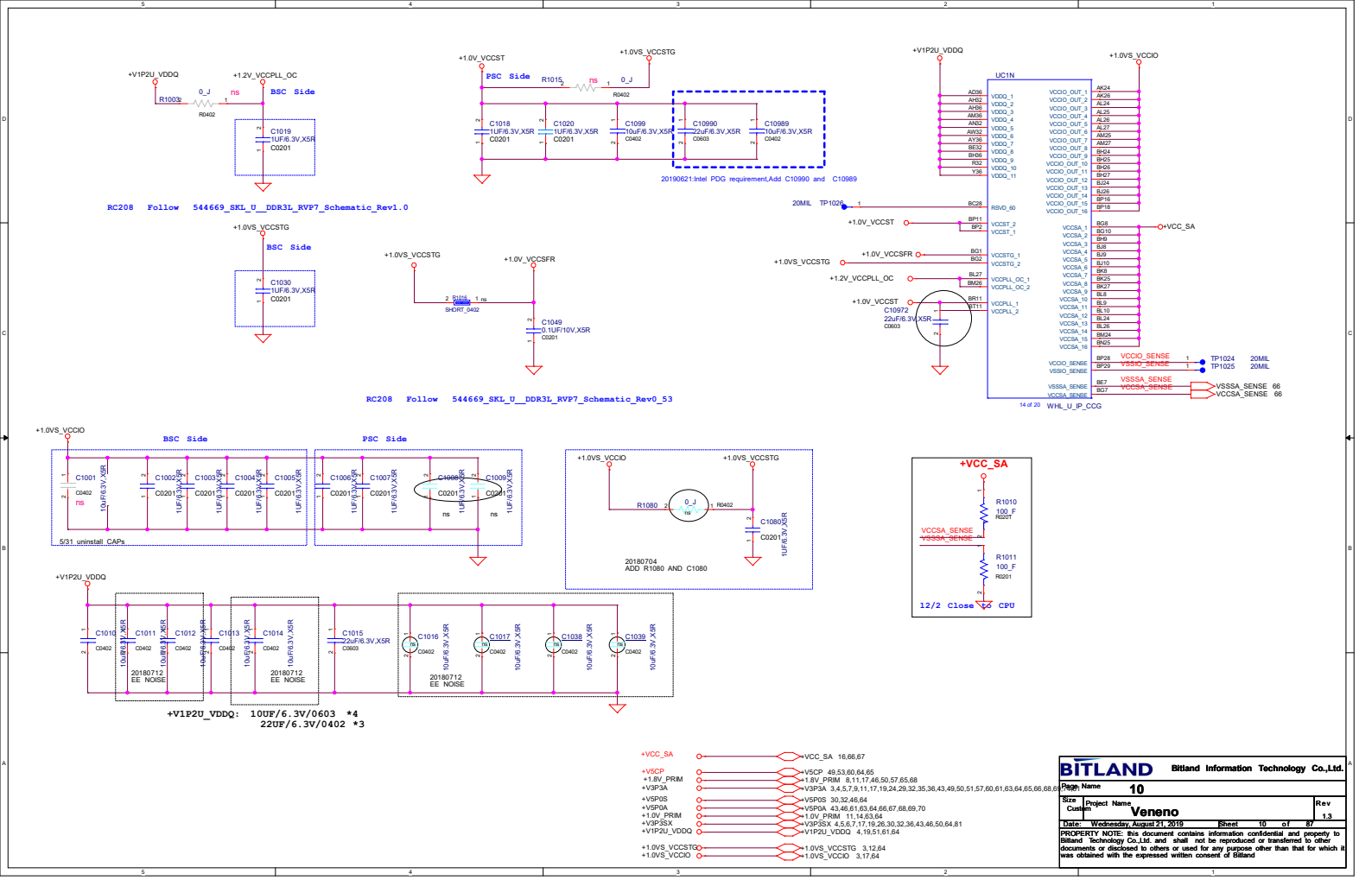

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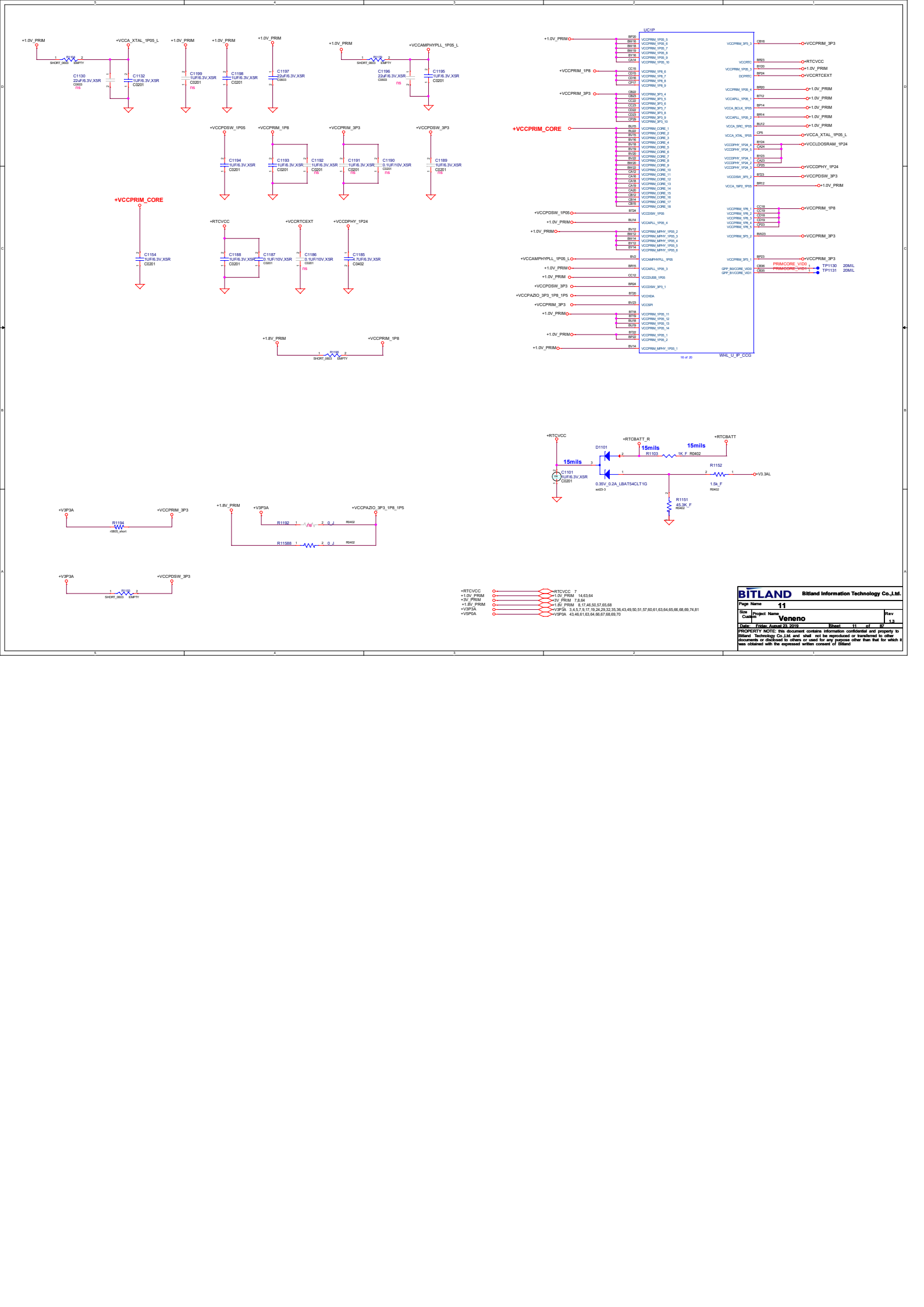

+RTCVCC	+RTCVCC_7	
+1.0V_PRIM	+1.0V_PRIM_14,63,64	
+3V_PRIM	+3V_PRIM_7,8,64	
+1.8V_PRIM	+1.8V_PRIM_8,17,46,50,57,65,68	
+V3P3A	+V3P3A_3,4,5,7,9,17,19,24,29,32,35,36,43,49,50,51,57,60,61,63,64,65,66,68,69,74,81	
+V5P0A	+V5P0A_43,46,61,63,64,66,67,68,69,70	

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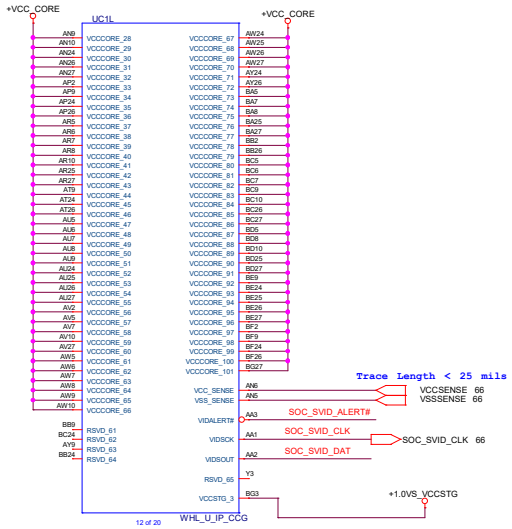
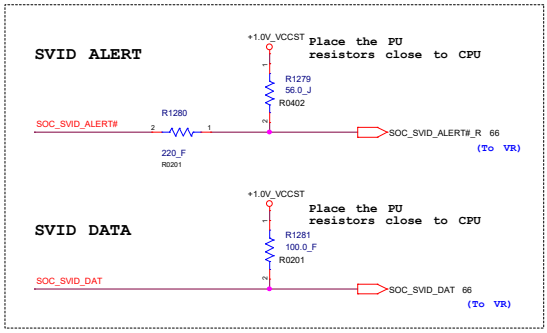
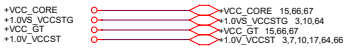
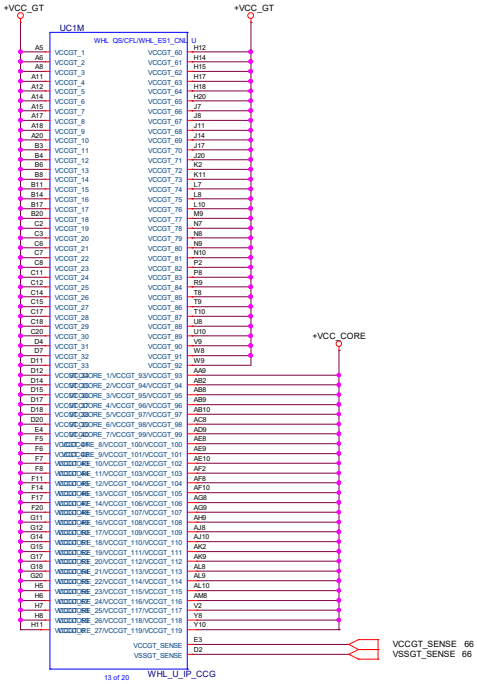
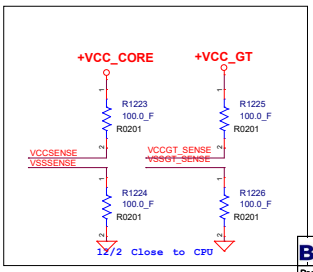








Trace Length < 25 mils



Package Sensing Recommendations

Power Rail Sense Line	R1, R2	Trace Impedance	Trace Length Match
V_{CC_SENSE} / V_{SS_SENSE}	100Ω	50Ω	<25 mils
$V_{CC_{GT}_SENSE}$ / $V_{SS_{GT}_SENSE}$			
$V_{CC_{GTx}_SENSE}$ / $V_{SS_{GTx}_SENSE}$			
$V_{CC_{SA}_SENSE}$ / $V_{SS_{SA}_SENSE}$			
$V_{CC_{IO}_SENSE}$ / $V_{SS_{IO}_SENSE}$[1]		NA	

Note: [1] Does not apply when rails are merged.

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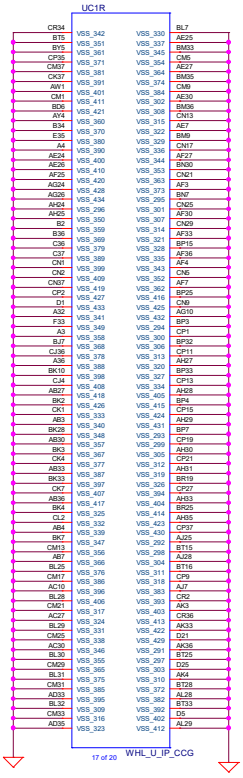

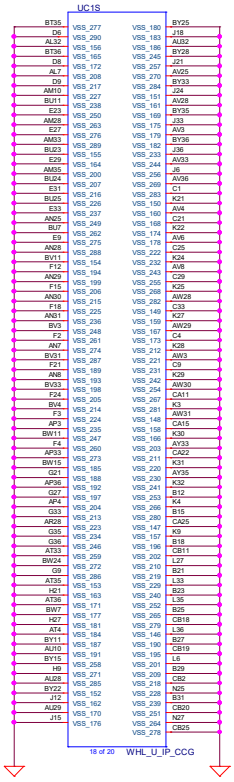

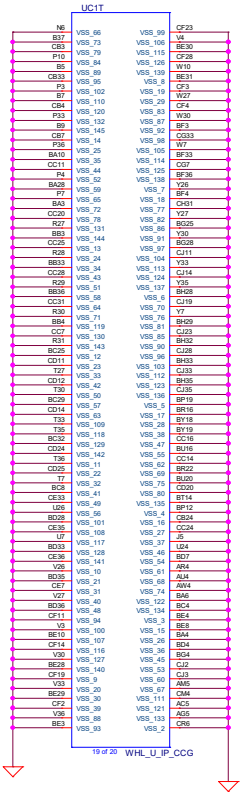

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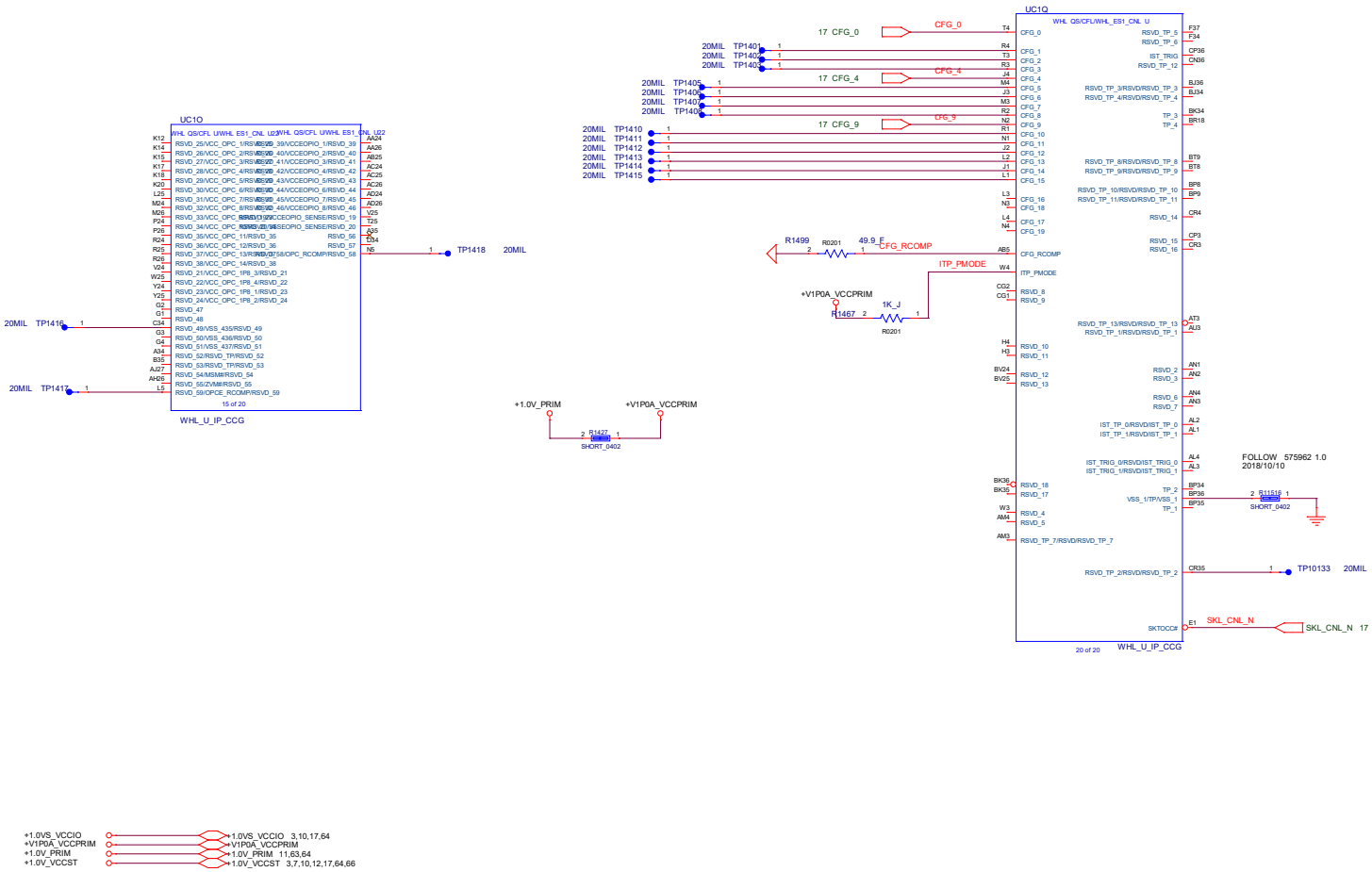

+1.0VS_VCCIO
+V1P0A_VCCPRIM
+1.0V_PRIM
+1.0V_VCCST

+1.0VS_VCCIO 3,10,17,64
+V1P0A_VCCPRIM
+1.0V_PRIM 11,63,64
+1.0V_VCCST 3,7,10,12,17,64,66

Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

Follow 544669_SKL_U_DDR3L_RVP7_schematic_rev1.0

For 2+3e Solution
PM_ZVM#
PM_MSM#

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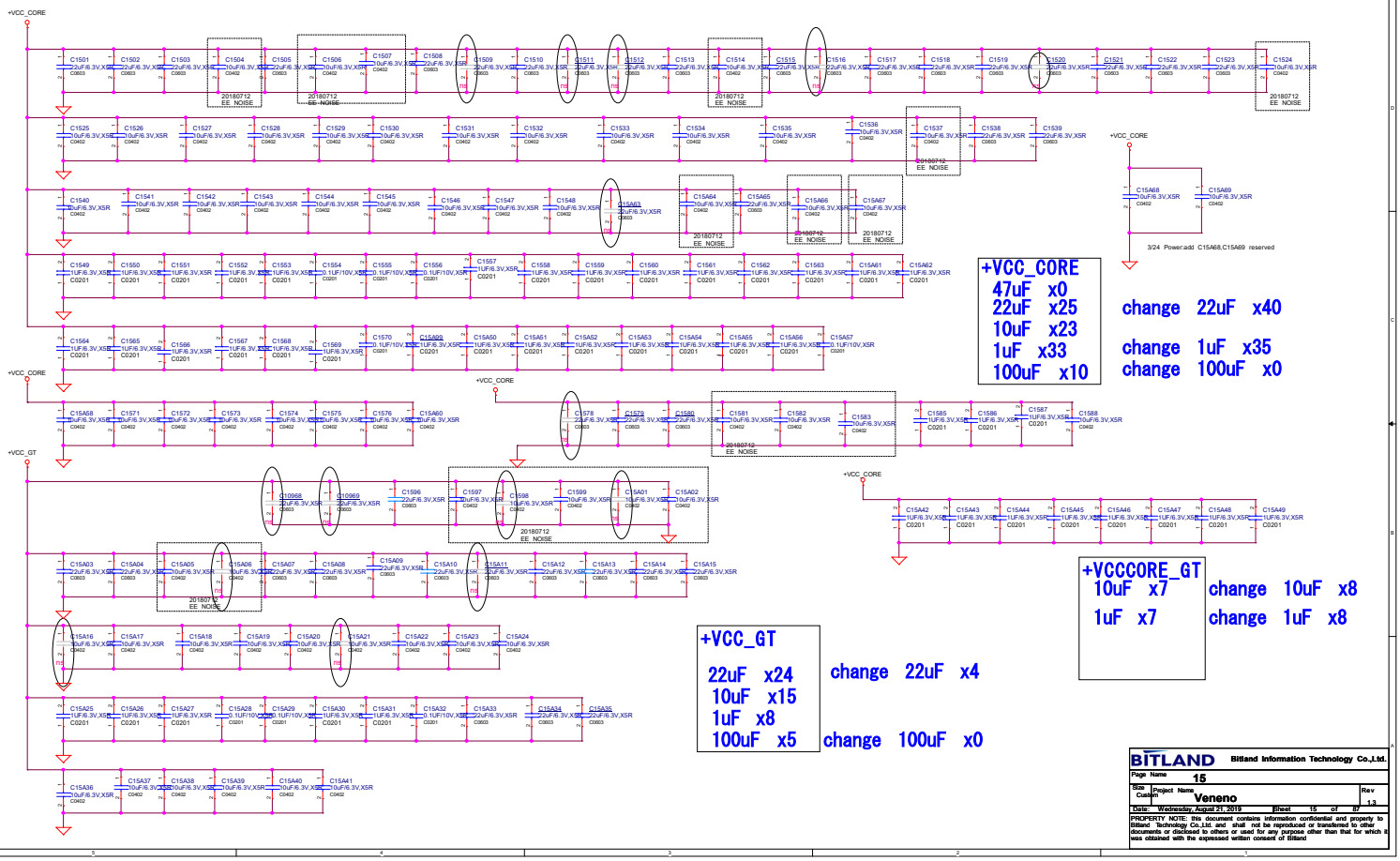

+VCC_CORE		
47uF	x0	
22uF	x25	change 22uF x40
10uF	x23	
1uF	x33	change 1uF x35
100uF	x10	change 100uF x0

+VCCCORE_GT		
10uF	x7	change 10uF x8
1uF	x7	change 1uF x8

+VCC_GT		
22uF	x24	change 22uF x4
10uF	x15	
1uF	x8	
100uF	x5	change 100uF x0

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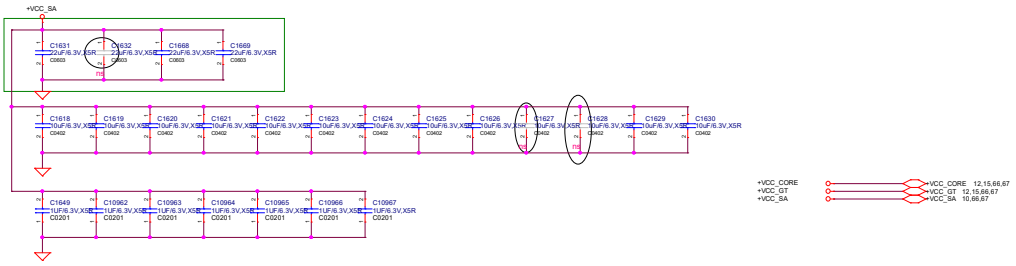

+VCC_SA
47uF x2
10uF x13
1uF x7

12/30 check PDG

+VCC_CORE
+VCC_GT
+VCC_SA

+VCC_CORE 12,15,66,67
+VCC_GT 12,15,66,67
+VCC_SA 10,66,67

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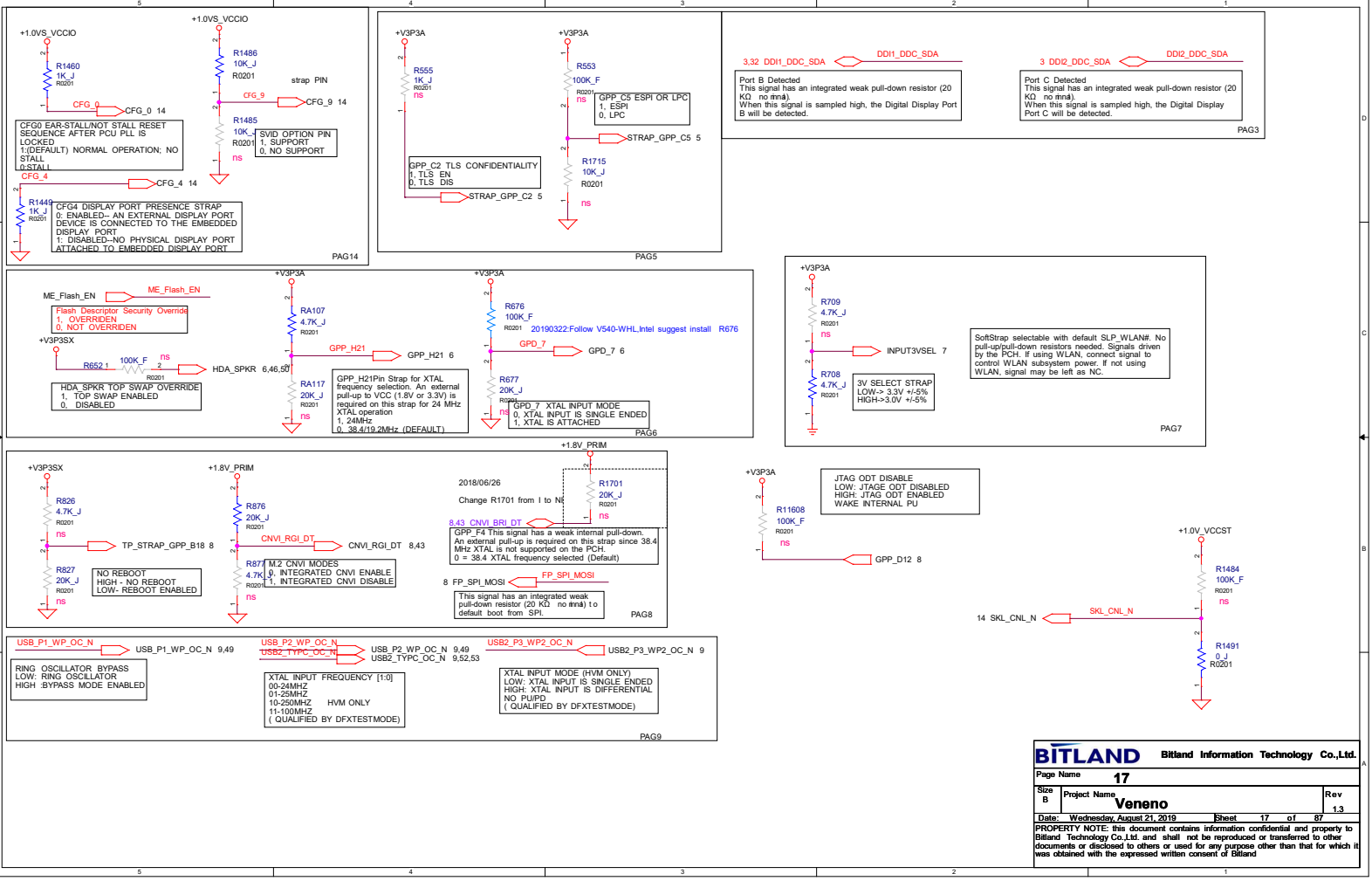

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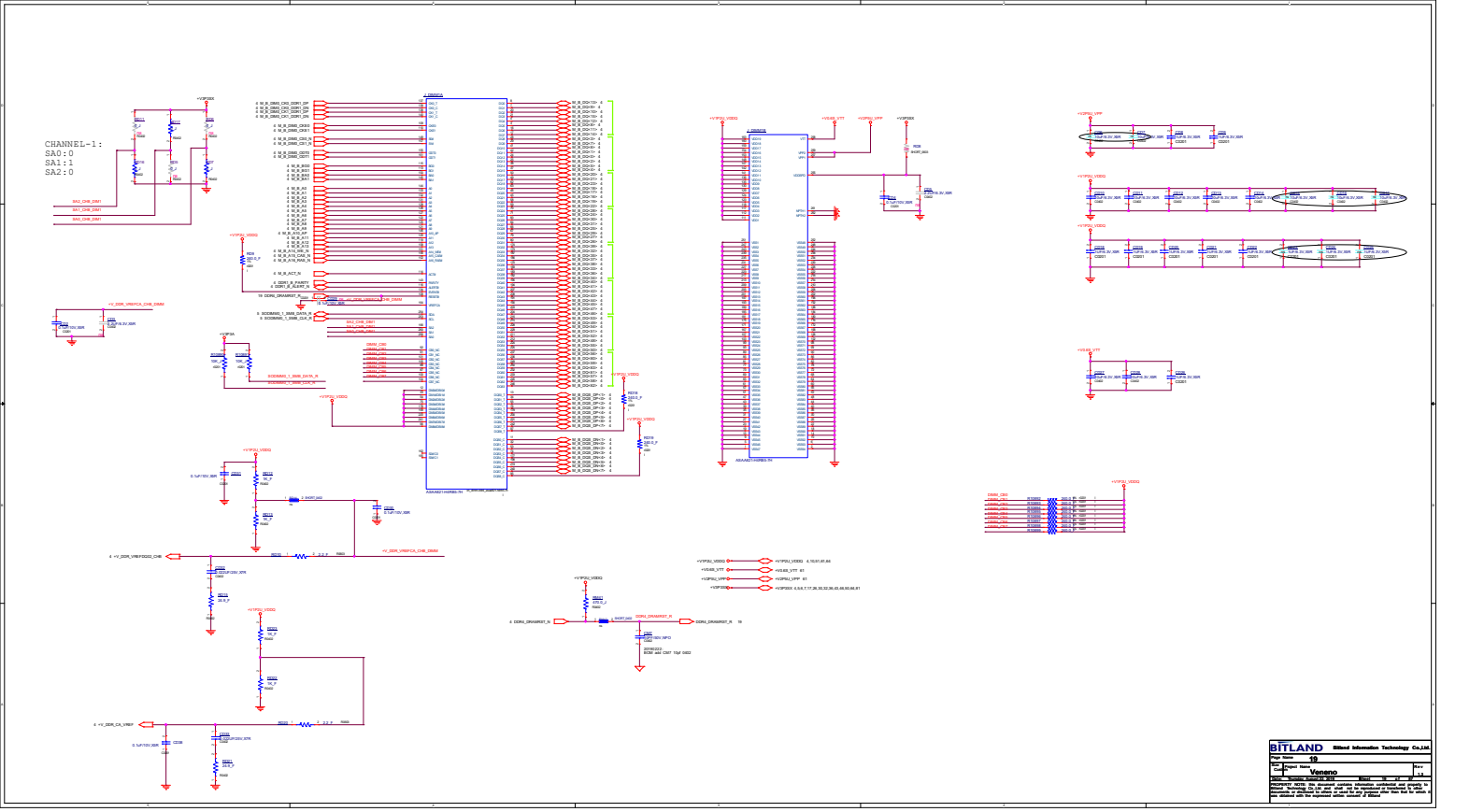

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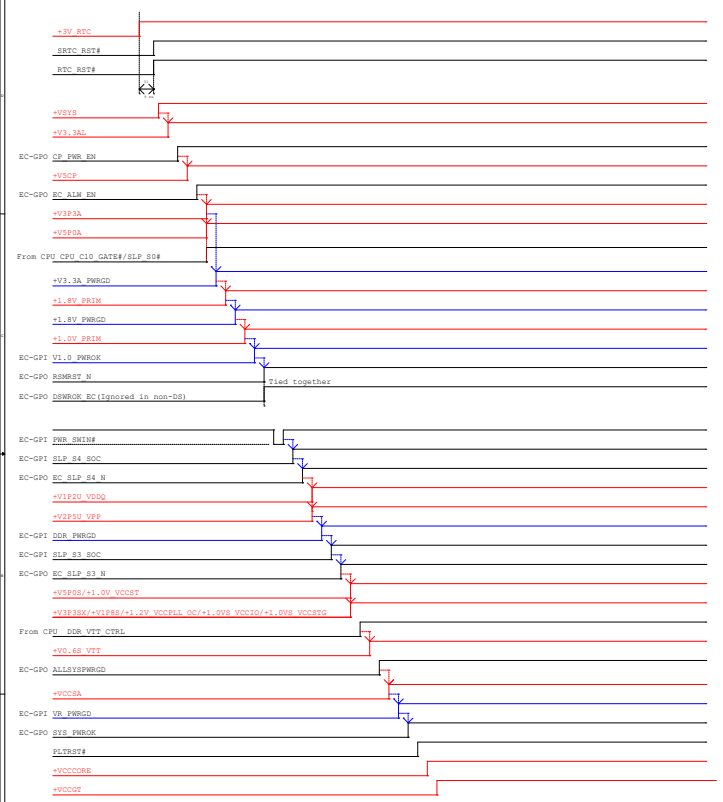
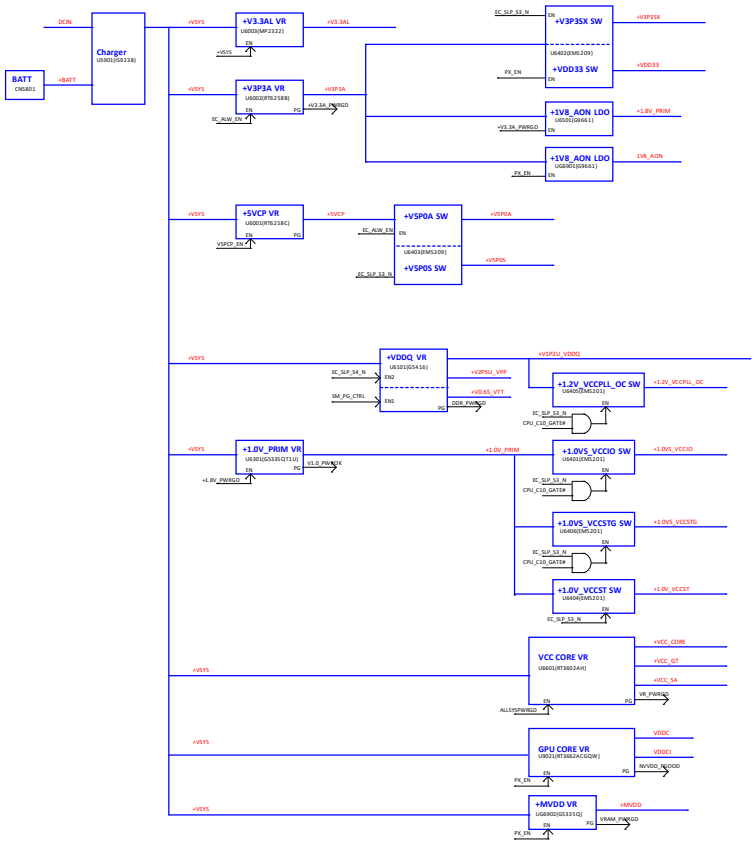
V540S Power Map





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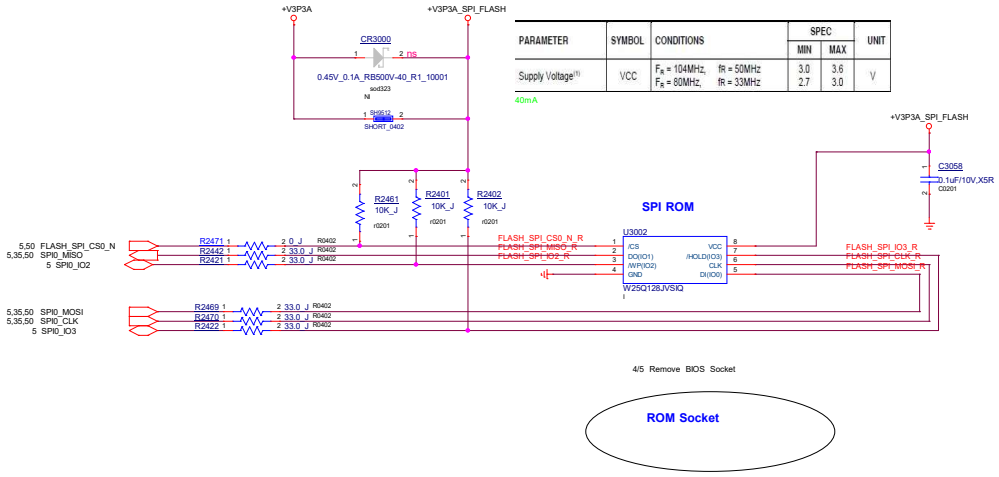

PARAMETER	SYMBOL	CONDITIONS	SPEC MIN	SPEC MAX	UNIT
Supply Voltage(1)	VCC	F_R = 104MHz, fR = 50MHz F_R = 80MHz, fR = 33MHz	3.0 2.7	3.6 3.0	V

40mA

4/5 Remove BIOS Socket

ROM Socket

2/24 SIV:Delet ROM Socket @U3002

+V3P3A → +V3P3A 3,4,5,7,9,11,17,19,29,32,35,36,43,49,50,51,57,60,61,63,64,65,66,68,69,74,81

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M.2 SSD Module

1.4A @ADATA 128GB SSD
2.6A @ADATA 256GB SSD

+V3P3SX — SH4200 (r0805_short) — +V3P3A_SSD

Change SH4200 0805 shunt to resistor

+V3P3A_SSD

C4209 22uF/6.3V,X5R C0603
C4204 22uF/6.3V,X5R C0603
C4205 0.1uF/10V,X5R C0201
C4206 0.1uF/10V,X5R C0201
C4207 0.1uF/10V,X5R C0201
C4208 0.1uF/10V,X5R C0201
ns

CIS ok

2/16 change CONN

JSSD1

9 PCIE9_SSD_RX_DN
9 PCIE9_SSD_RX_DP
9 PCIE9_SSD_TX_DN_C
9 PCIE9_SSD_TX_DP_C
9 PCIE10_SSD_RX_DN
9 PCIE10_SSD_RX_DP
9 PCIE10_SSD_TX_DN_C
9 PCIE10_SSD_TX_DP_C
9 PCIE11_SSD_RX_DN
9 PCIE11_SSD_RX_DP
9 PCIE11_SSD_TX_DN_C
9 PCIE11_SSD_TX_DP_C
9 PCIE12_SSD_RX_DP
9 PCIE12_SSD_RX_DN
9 PCIE12_SSD_TX_DN_C
9 PCIE12_SSD_TX_DP_C
7 PCIE_REFCLK_SSD_DN
7 PCIE_REFCLK_SSD_DP

R4200 1 2 SHORT_0402
R4201 1 2 SHORT_0402
PCIE12_SSD_RX_DP_R
PCIE12_SSD_RX_DN_R

GND_1 GND_3 PERp3 PERn3 GND_9 PETp3 PETn3 GND_15 PERp2 PERn2 GND_21 PETp2 PETn2 GND_27 PERp1 PERn1 GND_33 PETp1 PETn1 GND_39 PERp0/SATA-B+ PERn0/SATA-B- GND_45 PETn0/SATA-A- PETp0/SATA-A+ GND_51 REFCLKN REFCLKP GND_57

Key M

NC32 PEDET (OC-PCIe) GND_71 GND_73 GND_75

GND12 GND13 R2 R7

3.3V_2 3.3V_4 Reserved_6 Reserved_8 DAS/DSS# (O/OD) 3.3V_12 3.3V_14 3.3V_16 3.3V_18 Reserved_20 Reserved_22 Reserved_24 Reserved_26 Reserved_28 Reserved_30 Reserved_32 Reserved_34 Reserved_36 DEVSLP (I)(0/3.3V) Reserved_40 Reserved_42 Reserved_44 Reserved_46 Reserved_48 PERST# (I)(0/3.3V) CLKREQ# (IO)(0/3.3V) PEWake# (IO)(0/3.3V) Reserved_56 Reserved_58

SUSCLK(32kHz) (I)(0/3.3V) 3.3V_70 3.3V_72 3.3V_74

APCI0079-P002A

+V3P3A_SSD

R2626 10K_J r0201 — SATA2_DEVSLP 9

SSD_RST_R
SSD_CLK_REQ_N_R — RS13 R4206 0_J R0402 — SHORT_0402 — PLT_RST_N 7,35,43,50,74
M.2_SSD_PE_WAKE_N — R4205 0_J R0402 — SSD_CLK_REQ_N 7
PCIE_WAKE_PCH_N 7

2019022:
'SSD_RST_R' rise/fall is not monotonous
Add capacitance CS13 10PF/0402 at WIFI module side, and add RS13 33ohm 0402

+V3P3A_SSD — R4207 10K_J r0201 — SSD_RST_R — CS13 10PF/50V,NPO C0402

Pin54
PICE module spec is N/C
SATA module spec is N/C

PM_SUSCLK_SSD — TP9980

Pin68
PICE module spec is N/C
SATA module spec is N/C

+V3P3SX — R10869 20K_F R0402 — 9 SSD_SATA_PCIE_DET_N

Pin69
PICE module spec is 0
SATA module spec is 1

R10870 100K_F R0201 — ns

PCIE12 RX follow intel CRB

Difference with armour
SSD interface SATA change to PCIE
If install SATA CARD,R4200,R4201 need install 0.01uF
C0606,C0607 need install 0.01uF

Co-lay PCIE12 RX,reserved R4202,R4203 please close to R4200,R4201

+V3P3SX — +V3P3SX 4,5,6,7,17,19,30,32,36,43,46,50,64,81

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eky_y_nrd.+V3P3.26
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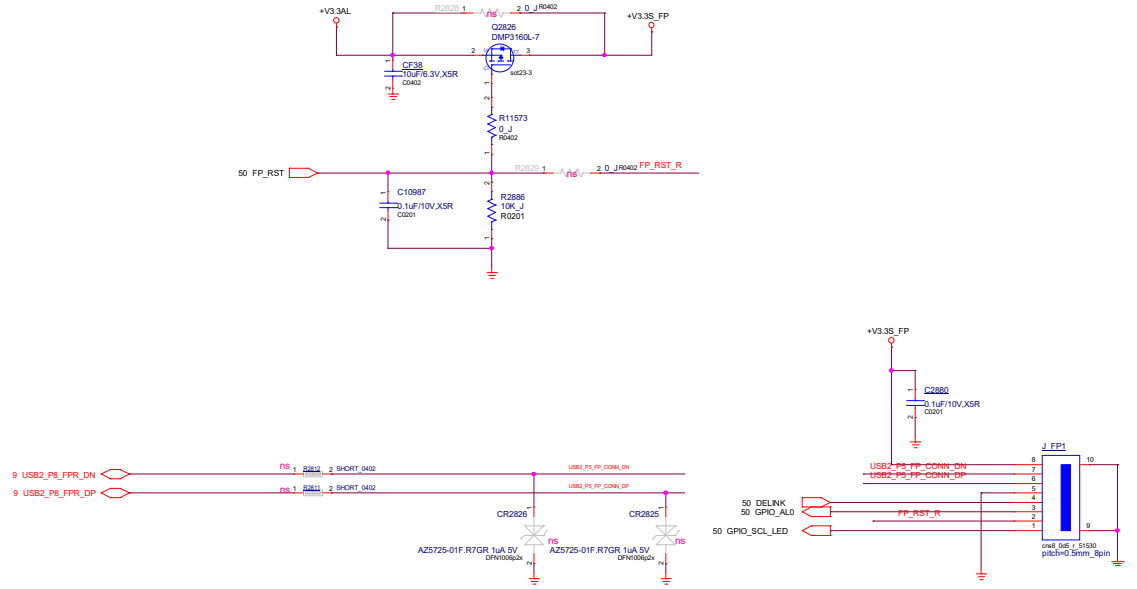

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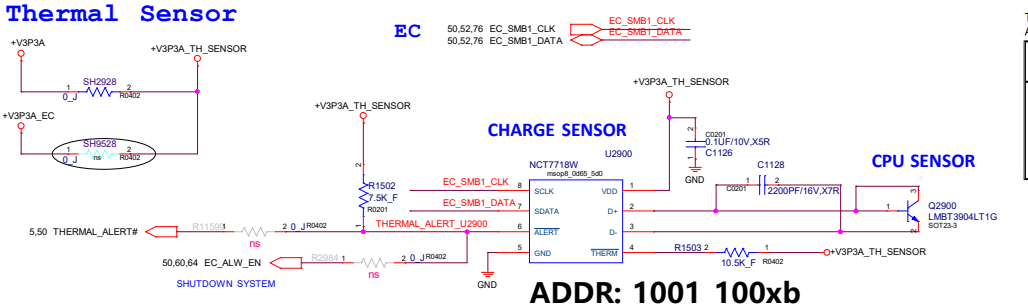
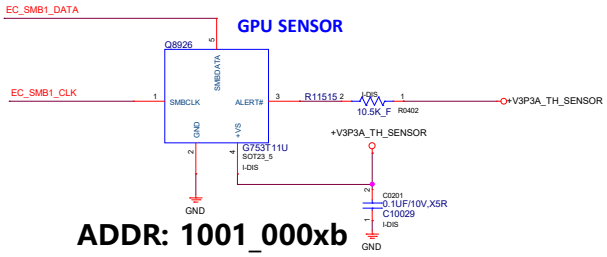
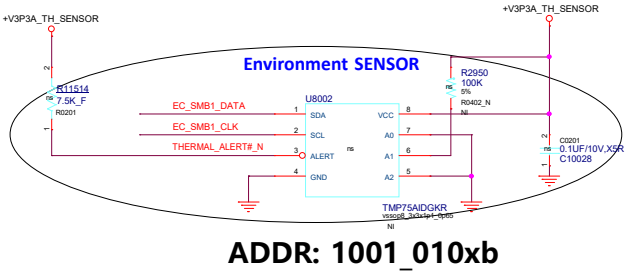
Thermal Sensor

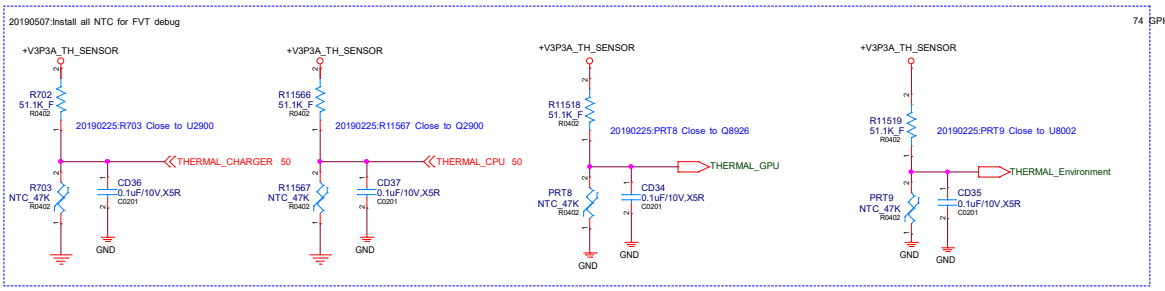


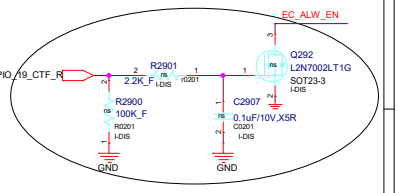
The default value is trapping after power up 100ms by different pull-up resistors of T_CRIT# and ALERT# pin:

TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125









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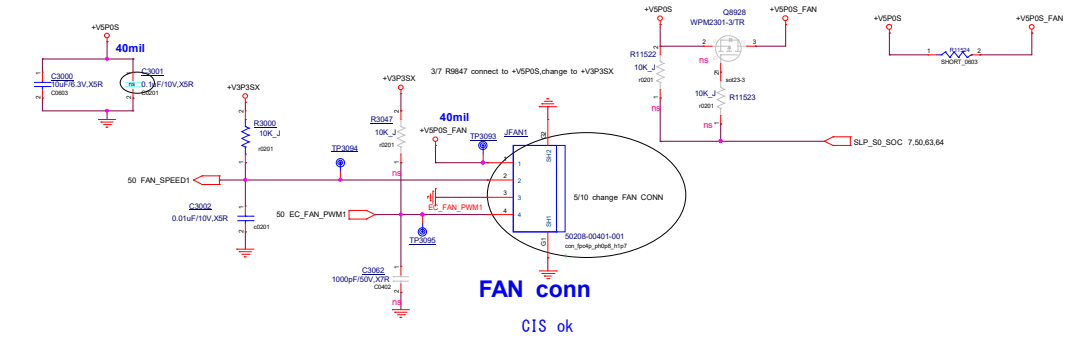

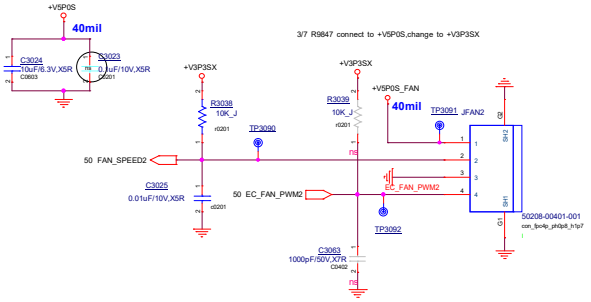

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HDMI Connector

for EMI Co-lay

3 DDI1_TX0_DP — C3201 — 0.1uF/10V,X5R C0201 — HDMI_TX2_CMC_DP — R3201 — 0_J R0402 — HDMI_TX2_DP
3 DDI1_TX0_DN — C3202 — 0.1uF/10V,X5R C0201 — HDMI_TX2_CMC_DN — R3202 — 0_J R0402 — HDMI_TX2_DN

20180711:Follow V540S-WHL change list
Change HDMI from 15R to 0R

3 DDI1_TX1_DP — C3203 — 0.1uF/10V,X5R C0201 — HDMI_TX1_CMC_DP — R3203 — 0_J R0402 — HDMI_TX1_DP
3 DDI1_TX1_DN — C3204 — 0.1uF/10V,X5R C0201 — HDMI_TX1_CMC_DN — R3210 — 0_J R0402 — HDMI_TX1_DN

3 DDI1_TX2_DP — C3205 — 0.1uF/10V,X5R C0201 — HDMI_TX0_CMC_DP — R3213 — 0_J R0402 — HDMI_TX0_DP
3 DDI1_TX2_DN — C3206 — 0.1uF/10V,X5R C0201 — HDMI_TX0_CMC_DN — R3214 — 0_J R0402 — HDMI_TX0_DN

3 DDI1_TX3_DP — C3207 — 0.1uF/10V,X5R C0201 — HDMI_CLK_CMC_DP — R3216 — 0_J R0402 — HDMI_CLK_DP
3 DDI1_TX3_DN — C3208 — 0.1uF/10V,X5R C0201 — HDMI_CLK_CMC_DN — R3217 — 0_J R0402 — HDMI_CLK_DN

HDMI_TX2_CMC_DP
HDMI_TX2_CMC_DN
HDMI_TX1_CMC_DP
HDMI_TX1_CMC_DN
HDMI_TX0_CMC_DP
HDMI_TX0_CMC_DN
HDMI_CLK_CMC_DP
HDMI_CLK_CMC_DN

R3208 R3209 R3204 R3205 R3211 R3212 R3206 R3207 — 270_J r0201
+V3P3SX
HDMI_PLS_FET
R10043 10K_J r0201
Q3201 L2N7002LT1G SOT23-3

FUSE need to be 1.1A

+V5P0S — R11520 0_J R0603 — F1 6V/1.1A fuse_1812 — +VHDMI

HDMI_TX2_DP
HDMI_TX2_DN
HDMI_TX1_DP
HDMI_TX1_DN
HDMI_TX0_DP
HDMI_TX0_DN
HDMI_CLK_DP
HDMI_CLK_DN
HDMI_CEC_1
HDMI_DDC_SCL
HDMI_DDC_SDA
HDMI_HPD

JHDMI1
D2+ D2 Shield D2- D1+ D1 Shield D1- D0+ D0 Shield D0- CK+ CK Shield CK- CE Remote NC DDC CLK DDC DATA GND +5V HP DET
SHELL1 SHELL2 SHELL3 SHELL4 G1 G2 G3 G4
30225-01902-001
on_hdmi-a_30225-00902-J01

TP10144

+VHDMI — C3209 1UF/10V,X5R C0402 — C3210 18PF/50V,NPO C0402

yangzw change 20180502

ESD3201
AZ1045-04F.R7G
lcc10_ns_2p5x1p0_p65h
EMC_NI

ESD3202
AZ1045-04F.R7G
lcc10_ns_2p5x1p0_p65h
EMC_NI

+V3P3A

R3219 10K_J r0201 — R3218 10K_J r0201 — Q3202B L2N7002DW1T1G SOT363
3 DDI1_DDC_SCK — DDI1_DDC_SCK
Q3202A L2N7002DW1T1G SOT363
3 DDI1_DDC_SDA — DDI1_DDC_SDA

+VHDMI — 0.45V_0.1A_RB500V-40_R1_10001 sod323 — D3201
RN_+VHDMI
R3221 10K_J r0201 — R3222 10K_J r0201 — C3211 1UF/10V,X5R C0402
HDMI_DDC_SCL
HDMI_DDC_SDA
CR3216 — AZ5825-01F 1uA 5V tvs_dfn1006p2x_0p5
CR3217 — AZ5825-01F 1uA 5V tvs_dfn1006p2x_0p5

+V3P3SX — R3220 1M_J r0201 — Q3203 L2N7002LT1G SOT23-3
3 DDI1_HPD — HDMI_HPD
C3212 1UF/10V,X5R C0402 — R3223 100K_F R0201
CR9053 — AZ5825-01F 1uA 5V tvs_dfn1006p2x_0p5

+V5P0S — +V5P0S 30,46,64
+V3P3SX — +V3P3SX 4,5,6,7,17,19,26,30,36,43,46,50,64,81
+V3P3A — +V3P3A 3,4,5,7,9,11,17,19,24,29,35,36,43,49,50,51,57,60,61,63,64,65,66,68,69,74,81

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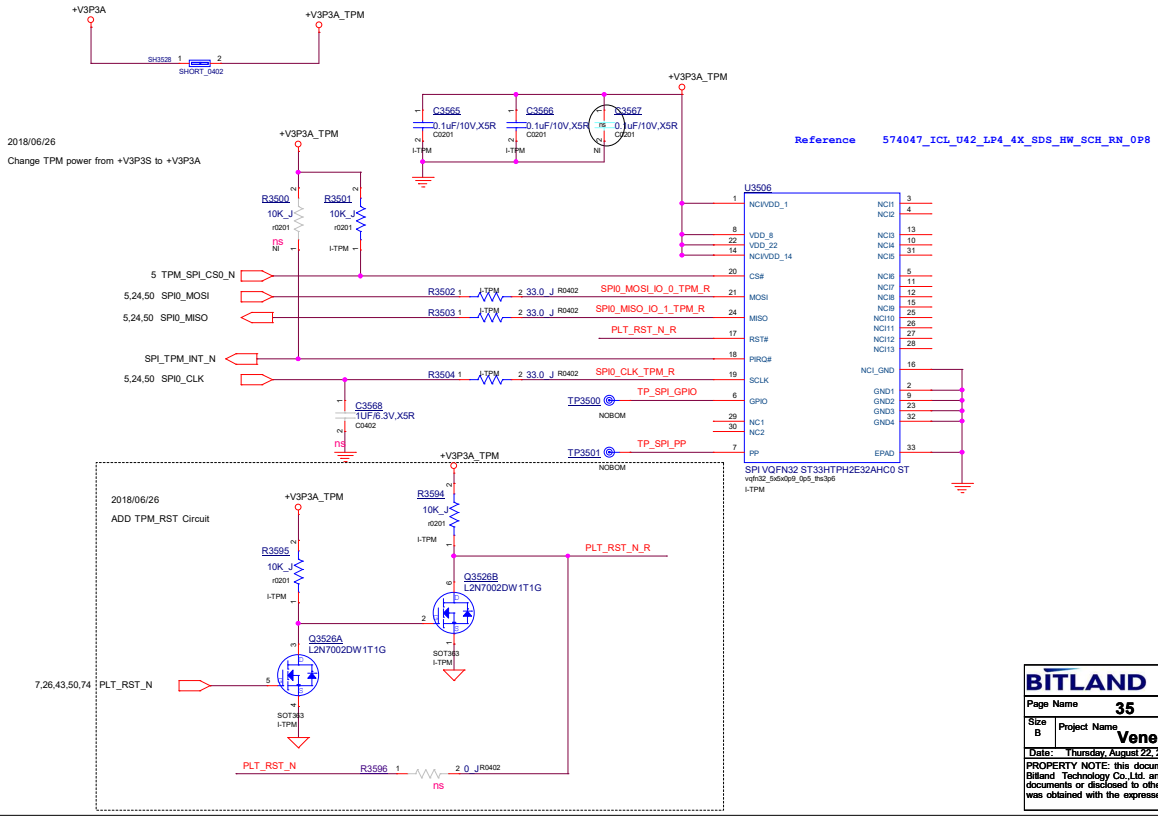
TPM 2.0



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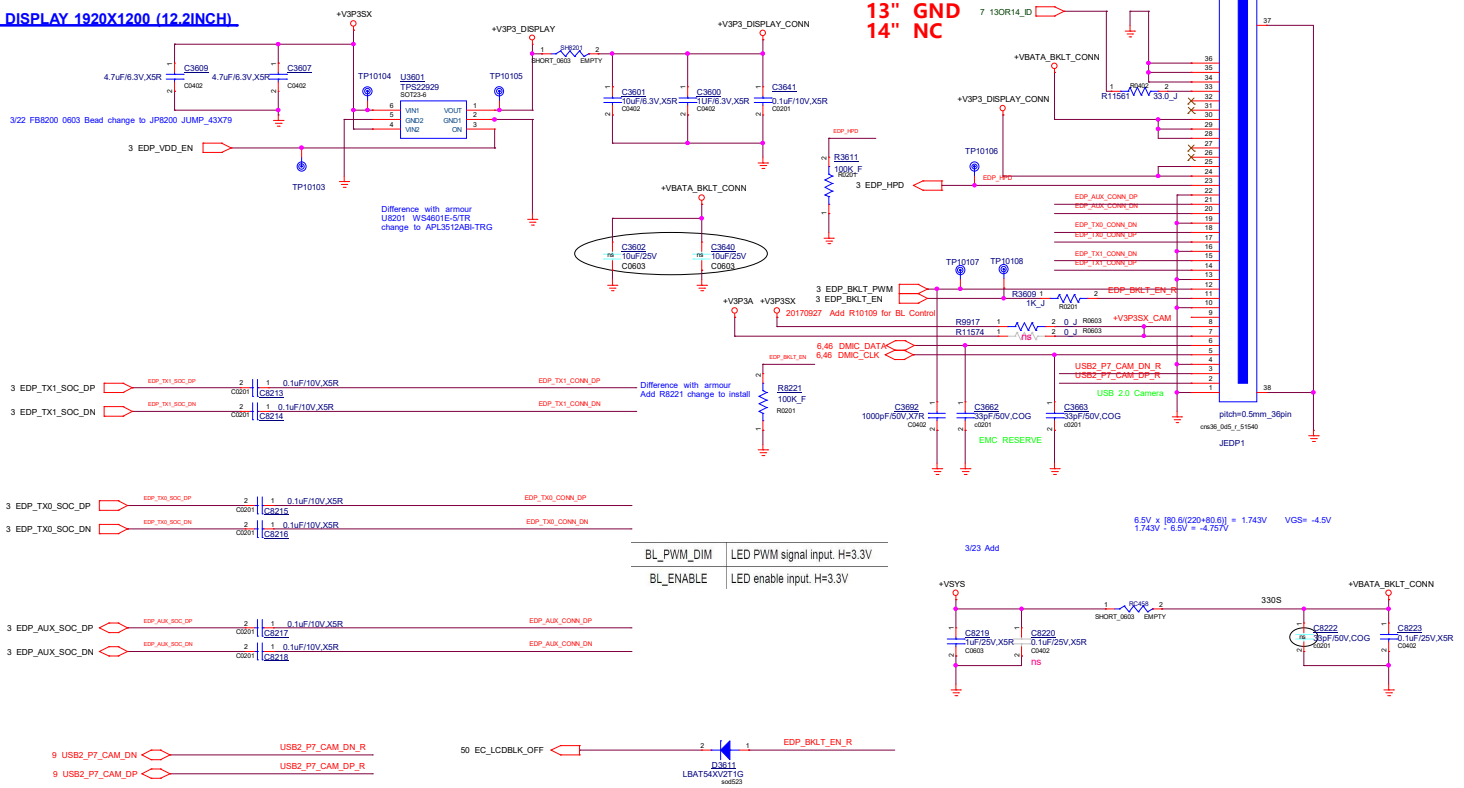
EDP DISPLAY 1920X1200 (12.2INCH)



BL_PWM_DIM	LED PWM signal input. H=3.3V
BL_ENABLE	LED enable input. H=3.3V

6.5V x [80.6/(220+80.6)] = 1.743V VGS= -4.5V
1.743V - 6.5V = -4.757V

3/23 Add

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USB2.0

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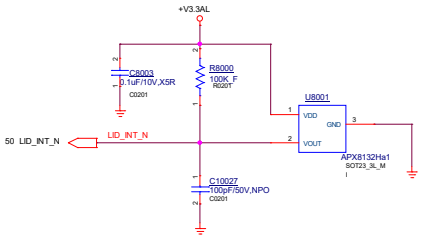
LID Sensor

Working voltage 2.4/ 2.7/ 5.5
max current 2.5mA typ:3uA



+V3.3ALO +V3.3AL 11,28,49,50,58,60

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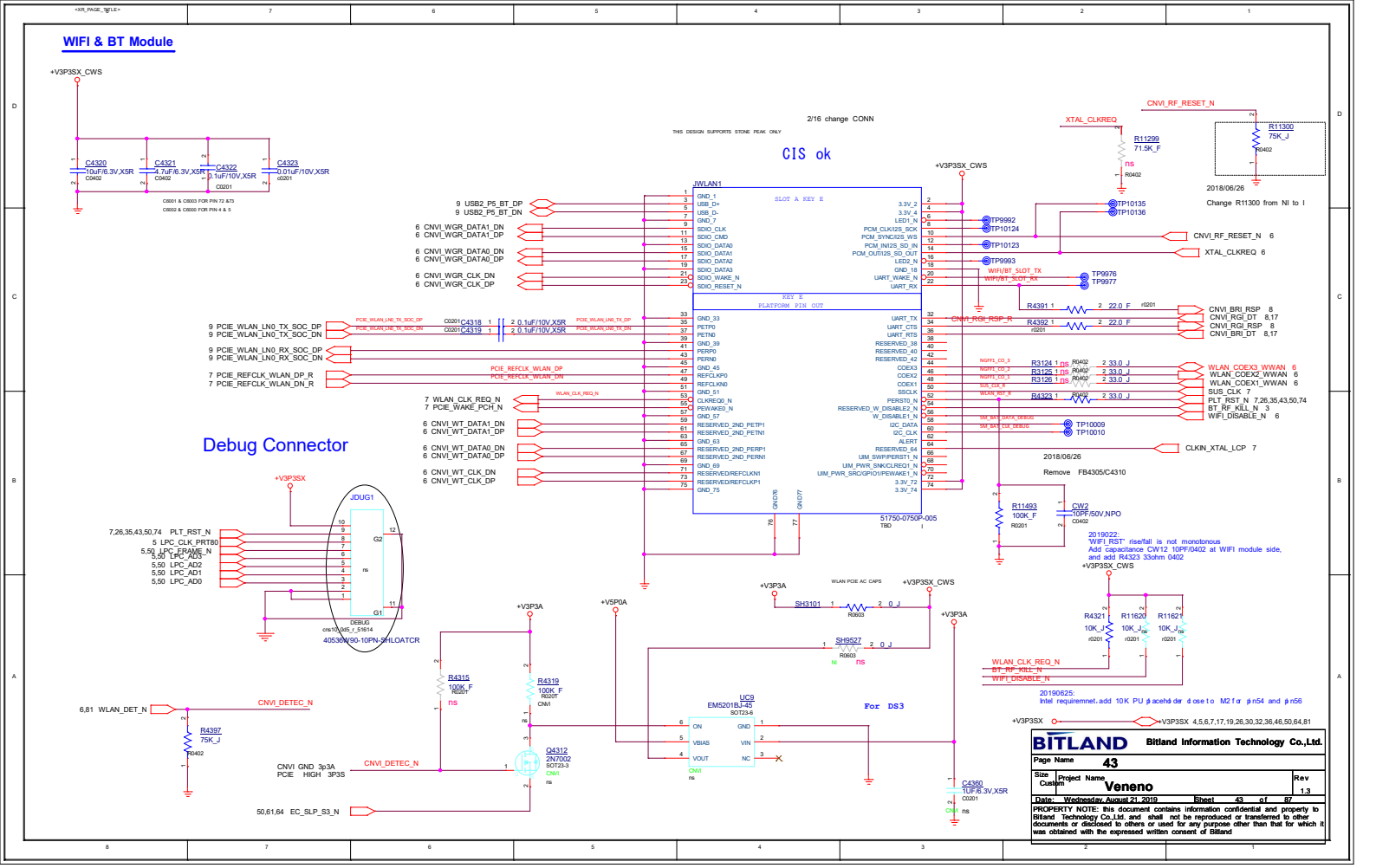
WIFI & BT Module
Debug Connector
CIS ok
2/16 change CONN
THIS DESIGN SUPPORTS STONE PEAK ONLY
JWLAN1
SLOT A KEY E
KEY E
PLATFORM PIN OUT
51750-0750P-005
JDUG1
DEBUG
40530W90-10PN-SHLOATCR
UC9
EM5201BJ-45
SOT23-6
Q4312
2N7002
SOT23-3
For DS3
2018/06/26
Change R11300 from NI to I
2018/06/26
Remove FB4305/C4310
2019022:
'WIFI_RST' rise/fall is not monotonous
Add capacitance CW12 10PF/0402 at WIFI module side,
and add R4323 33ohm 0402
20190625:
Intel requiremnet, add 10K PU placehold der close to M2 for pin54 and pin56
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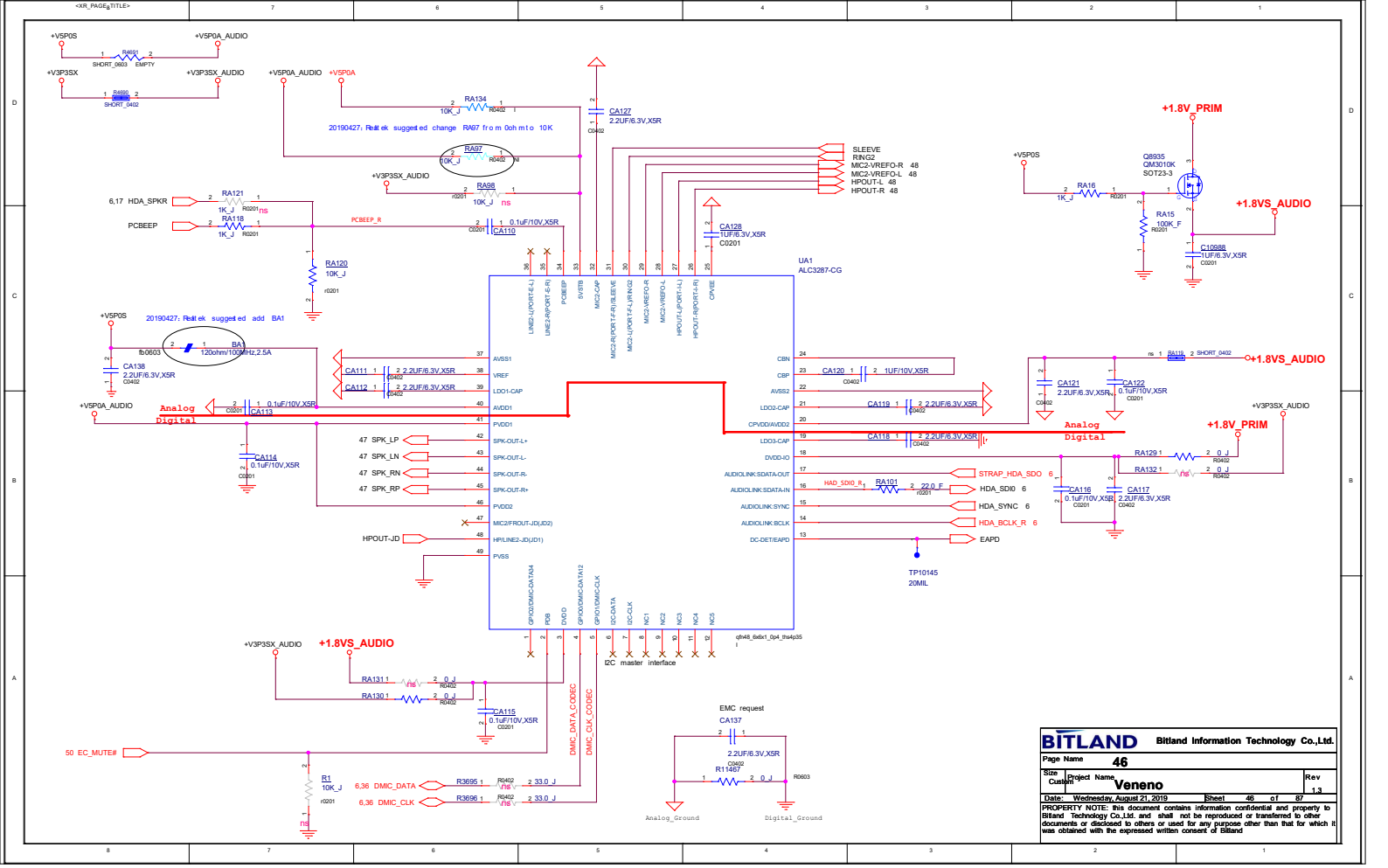

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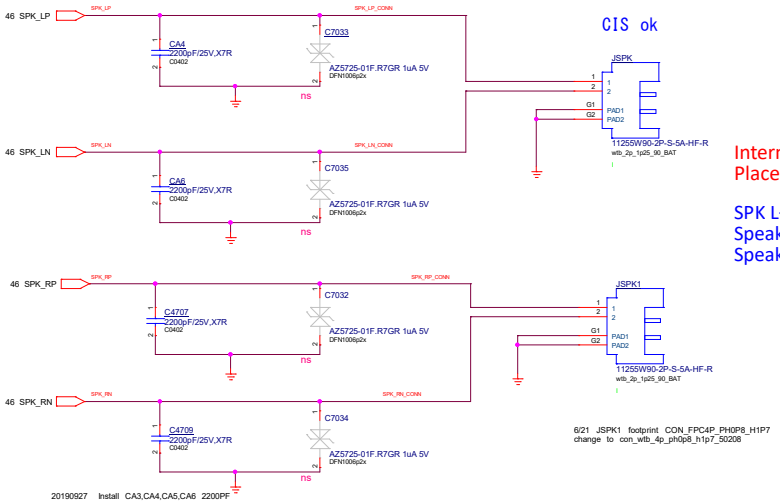
Speaker



20190927 Install CA3,CA4,CA5,CA6 2200PF

6/21 JSPK1 footprint CON_FPC4P_PH0P8_H1P7
change to con_wtb_4p_ph0p8_h1p7_50208

Internal Speaker connector
Placement near Audio Codec

SPK L+ L- R+ R- trace width
Speaker 4 ohm ==> 40 mils
Speaker 8 ohm ==> 20 mils

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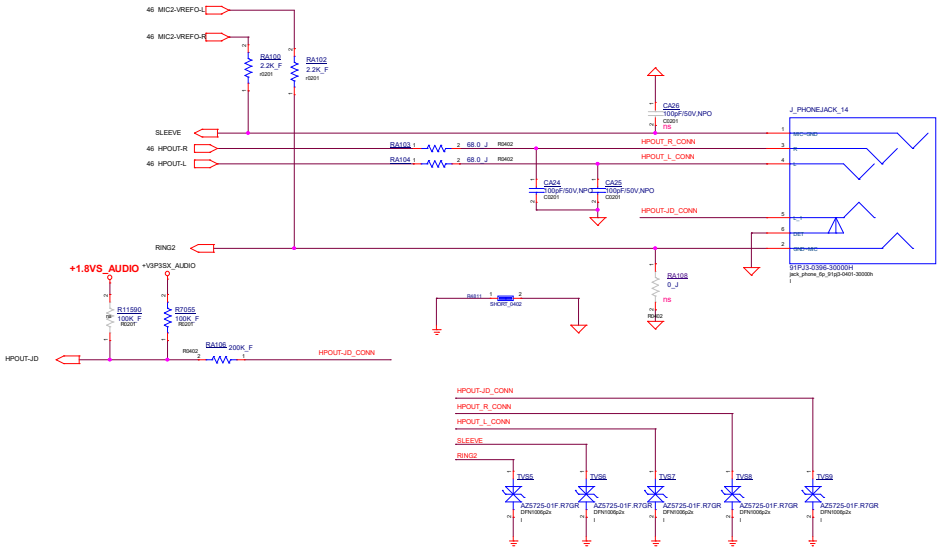
HEADSET JACK (Supports CTIA and OMTP headsets)

Important:
To ensure reliable headset detection for all fast/slow plug-in scenarios use a jack with the detect switch all the way at the end so that the switch is tripped only when the jack is plugged all the way in.



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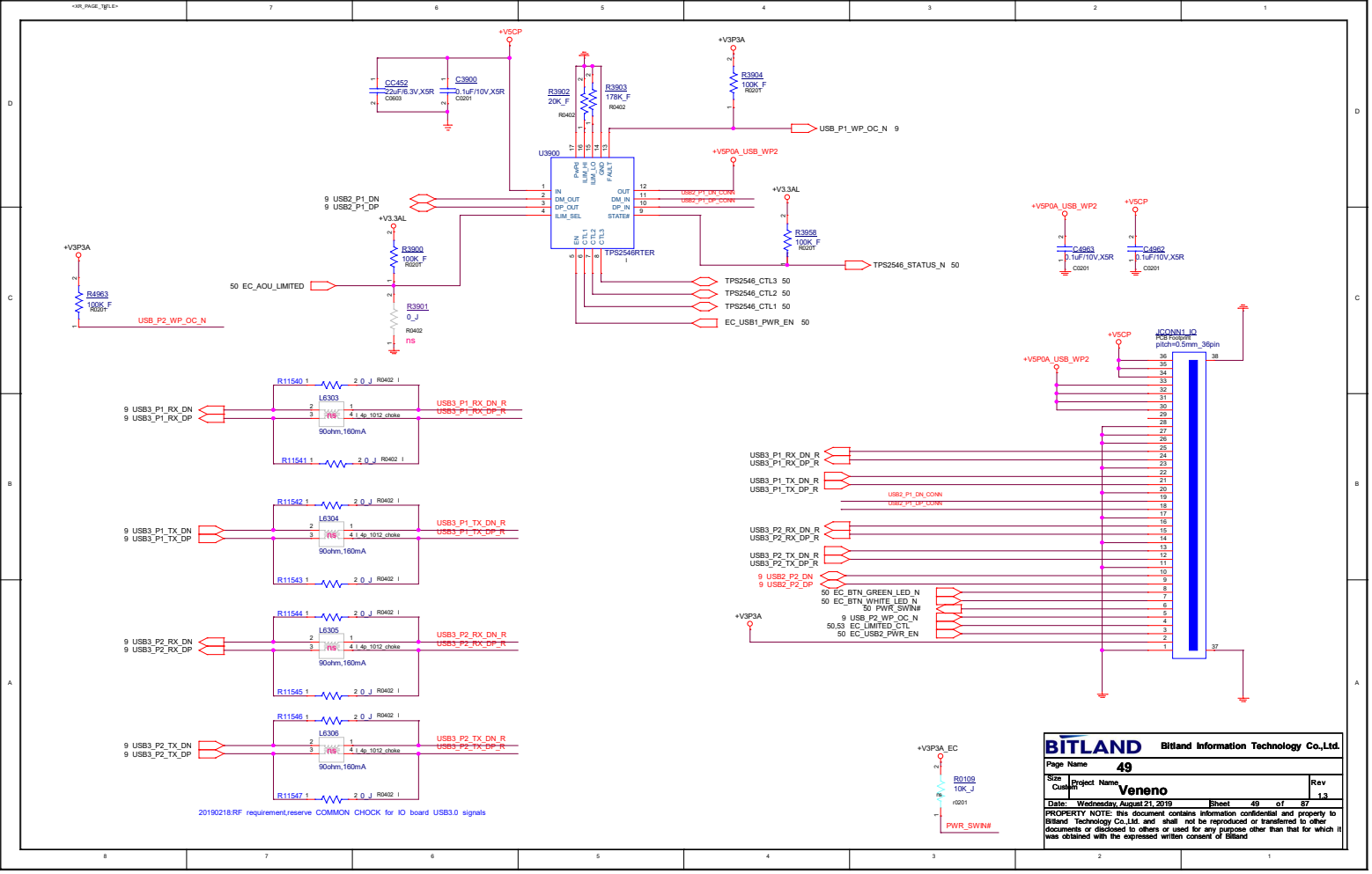

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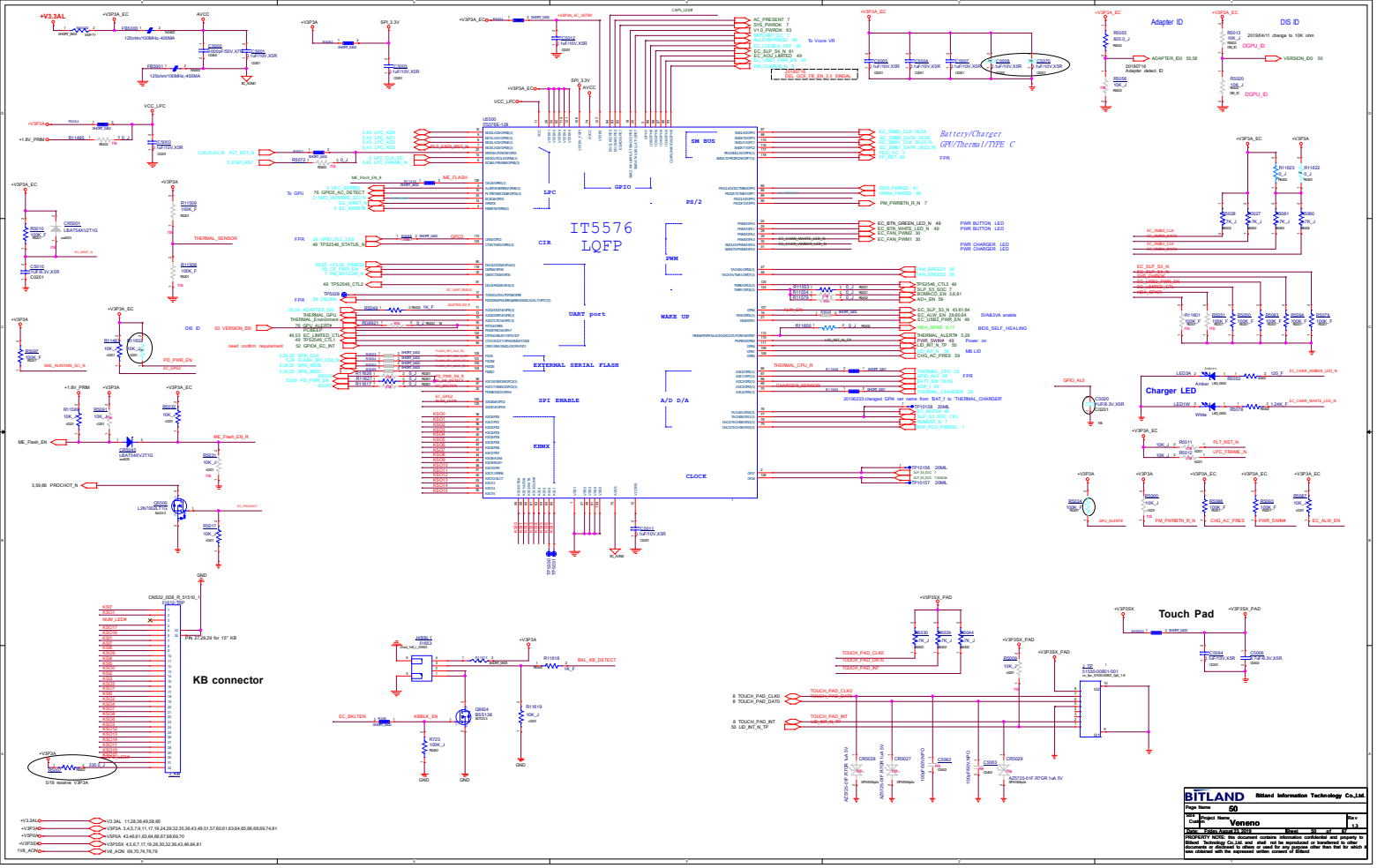

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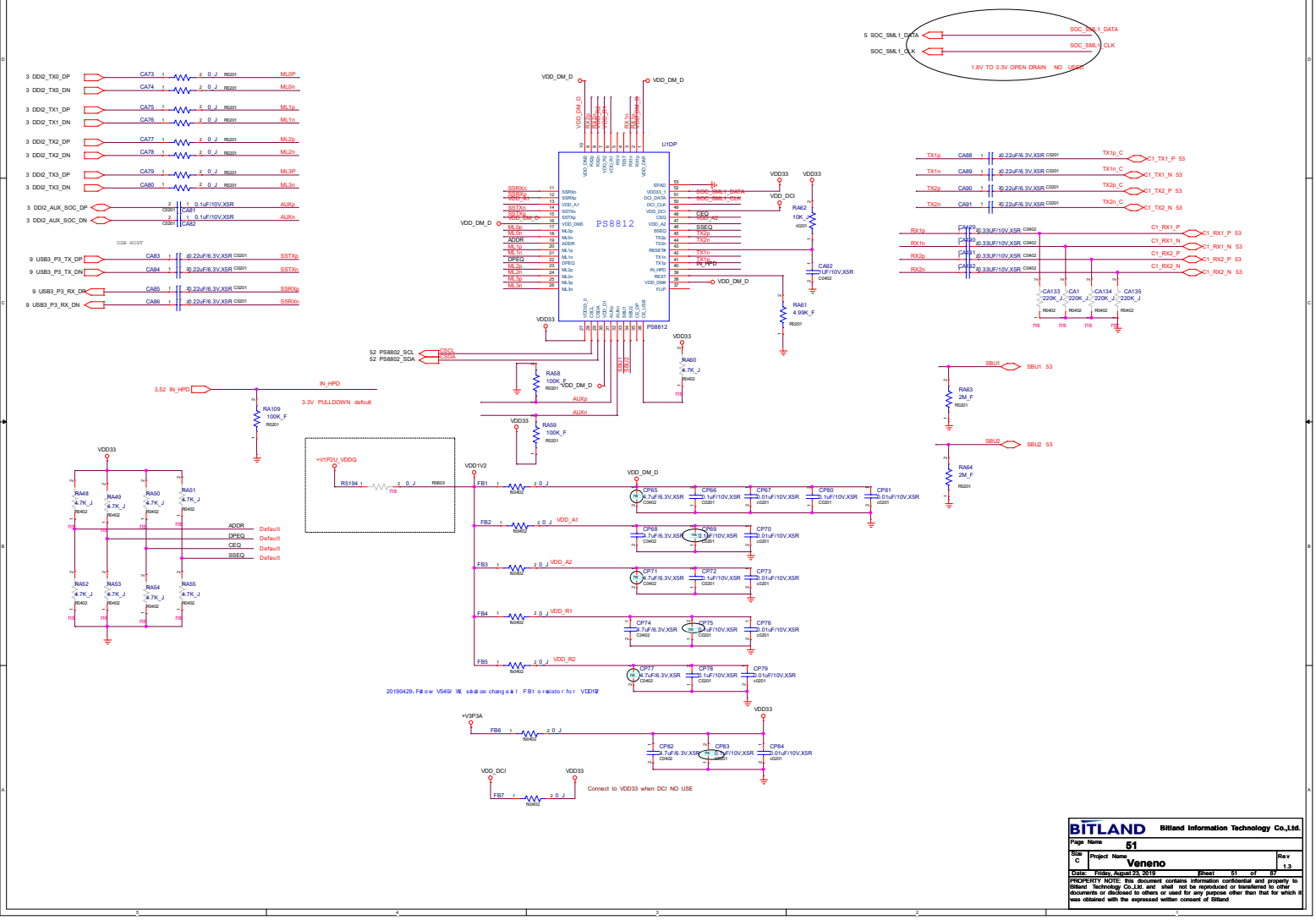

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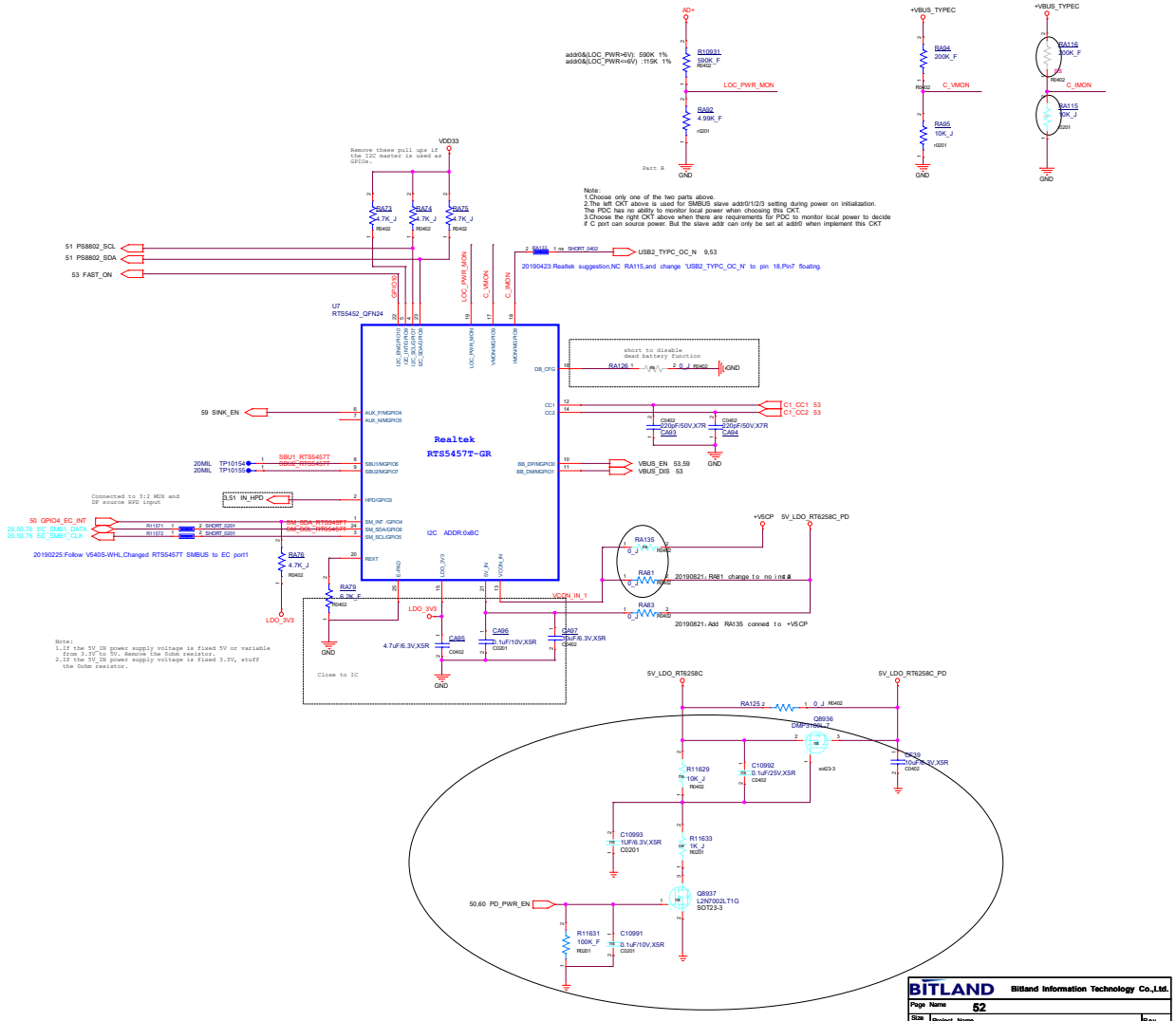

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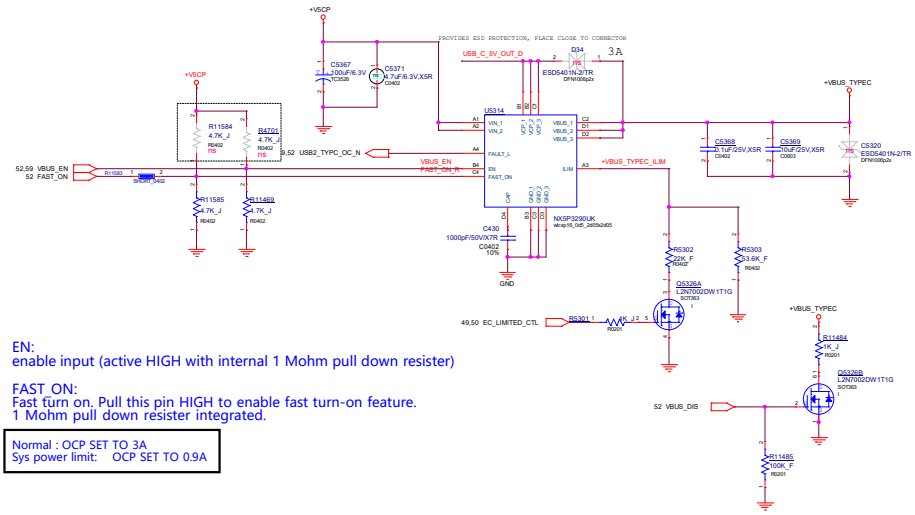
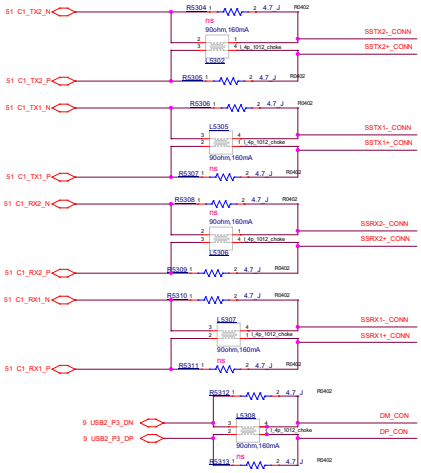
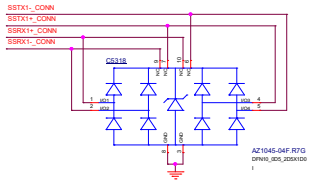


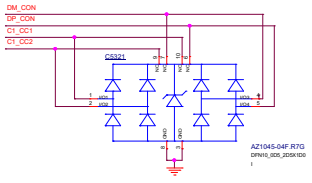
EN:
enable input (active HIGH with internal 1 Mohm pull down resister)

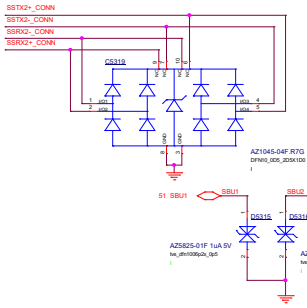
FAST_ON:
Fast turn on. Pull this pin HIGH to enable fast turn-on feature.
1 Mohm pull down resister integrated.

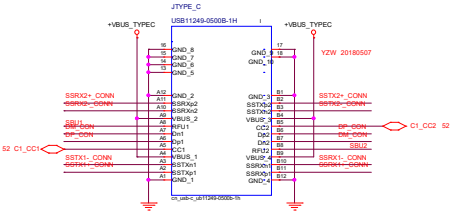
Normal : OCP SET TO 3A
Sys power limit: OCP SET TO 0.9A











+VBUS_TYPEC +VBUS_TYPEC 52,59

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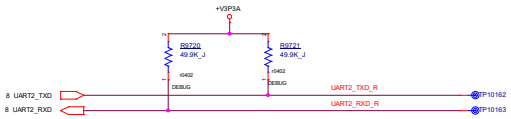
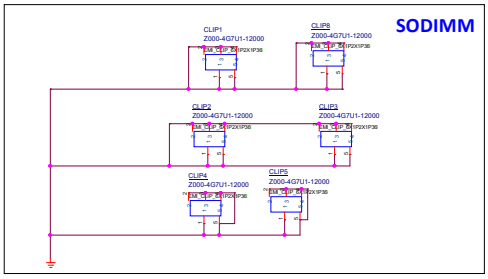
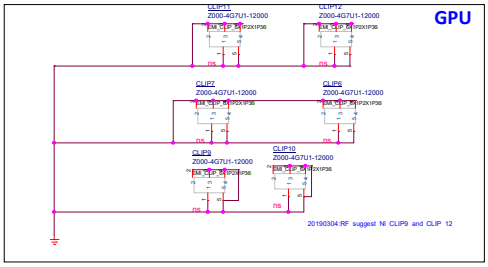
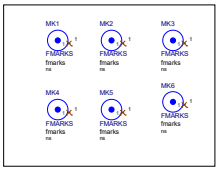


DEBUG CONN

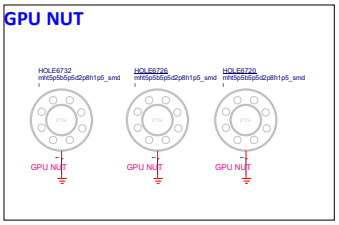
Shielding

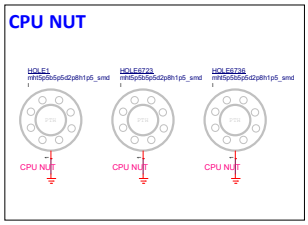


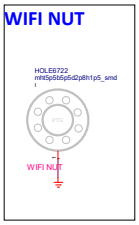




Holes







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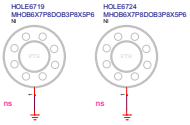

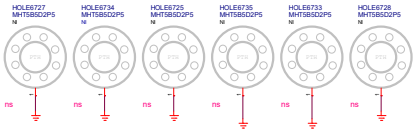

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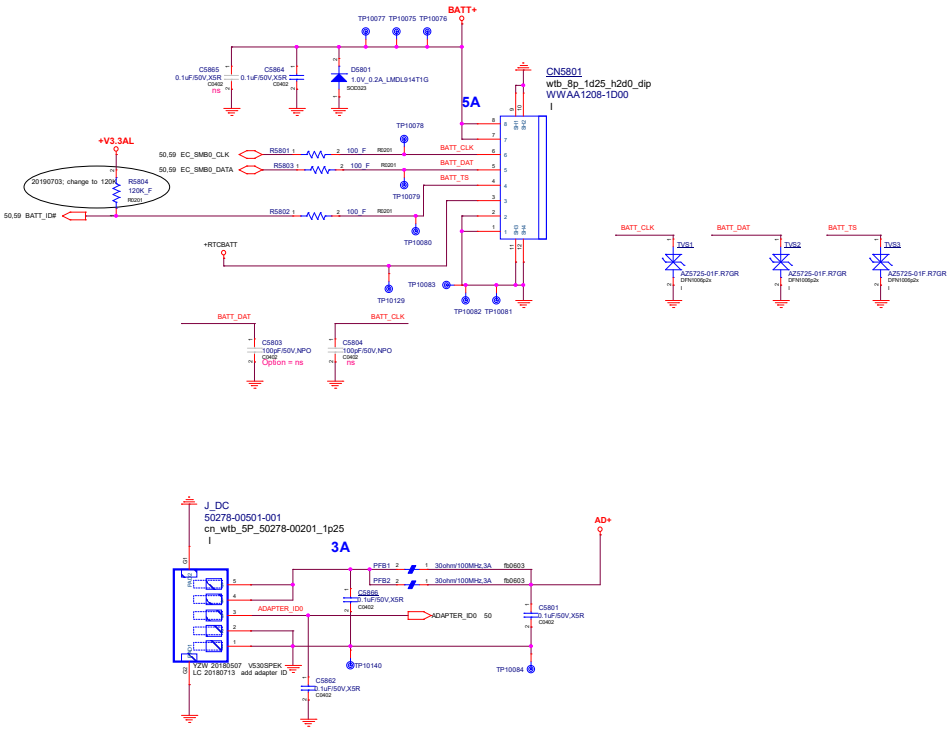
58: BATTERY CONNECTOR

BATT+ BATT+ 59
+V3.3AL +V3.3AL 11,28,38,49,50,60
DCIN DCIN 59



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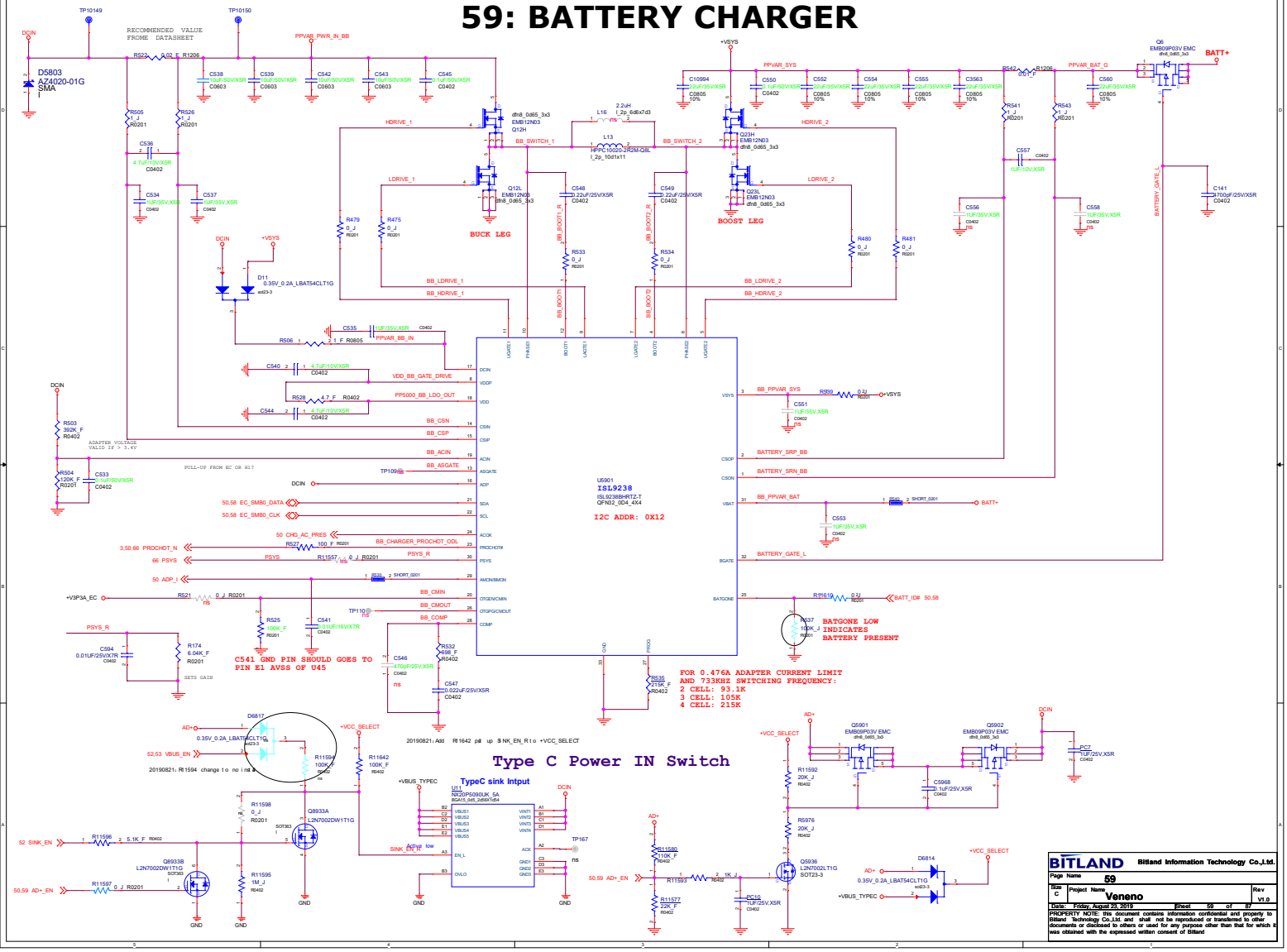
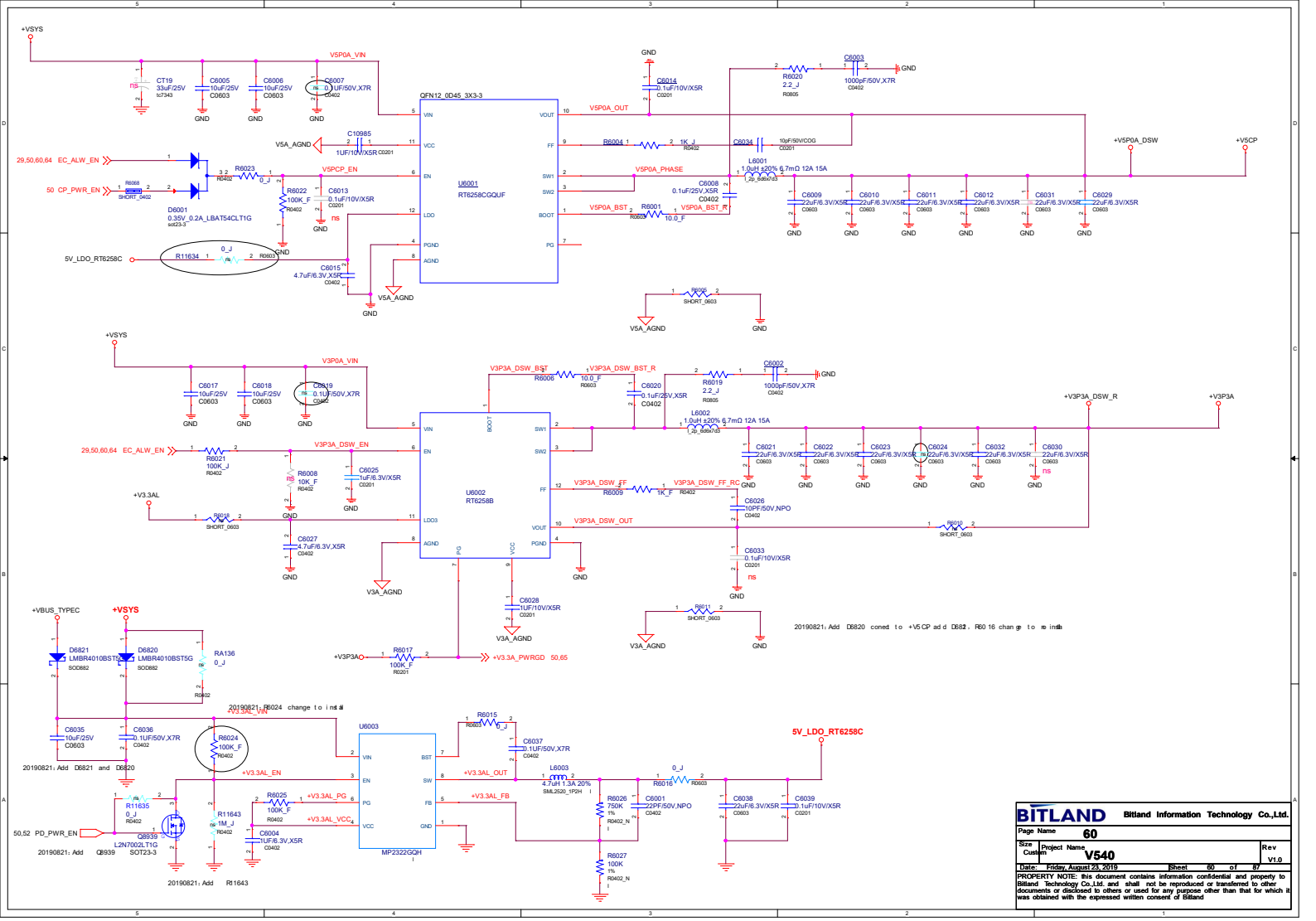
59: BATTERY CHARGER





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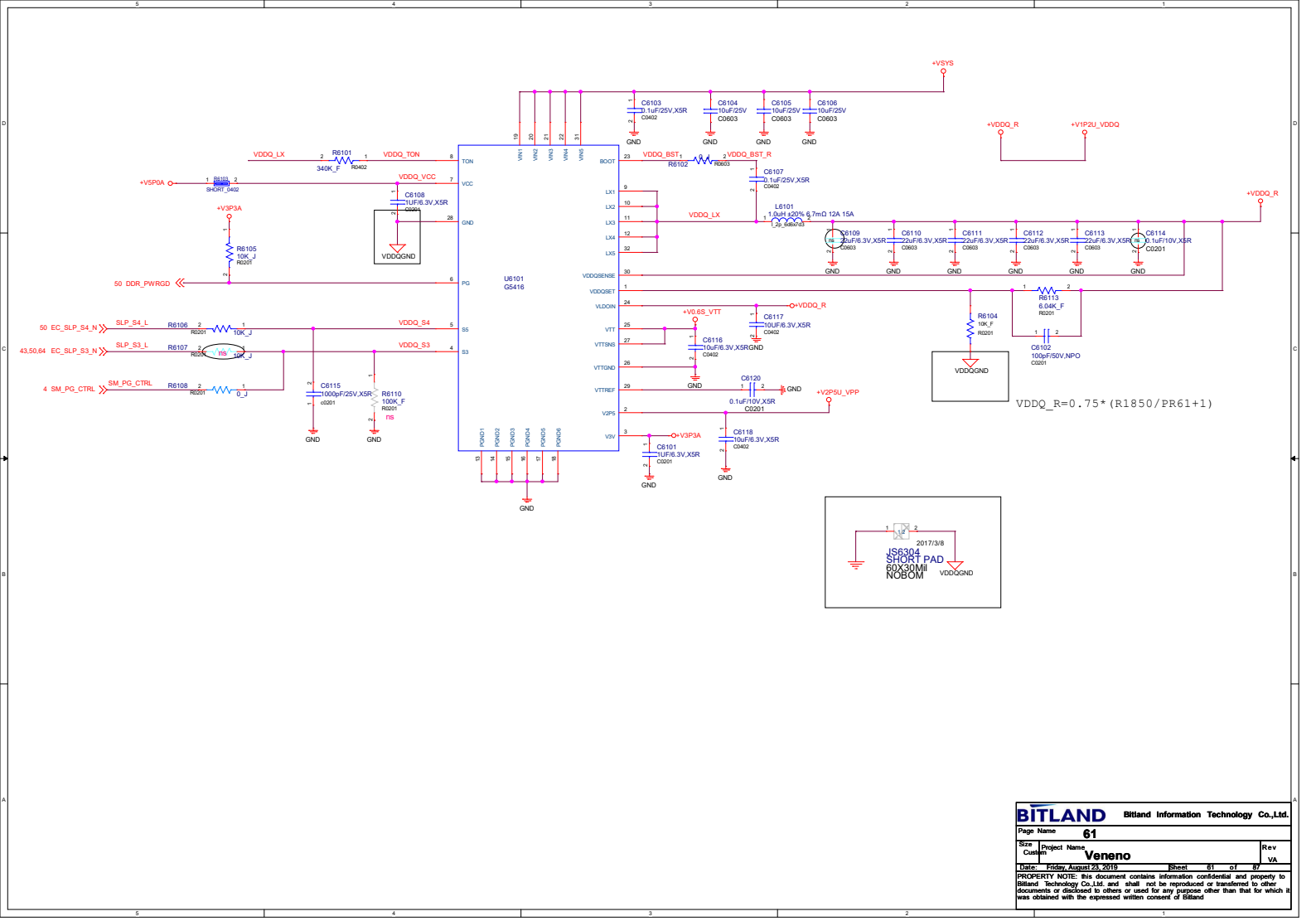

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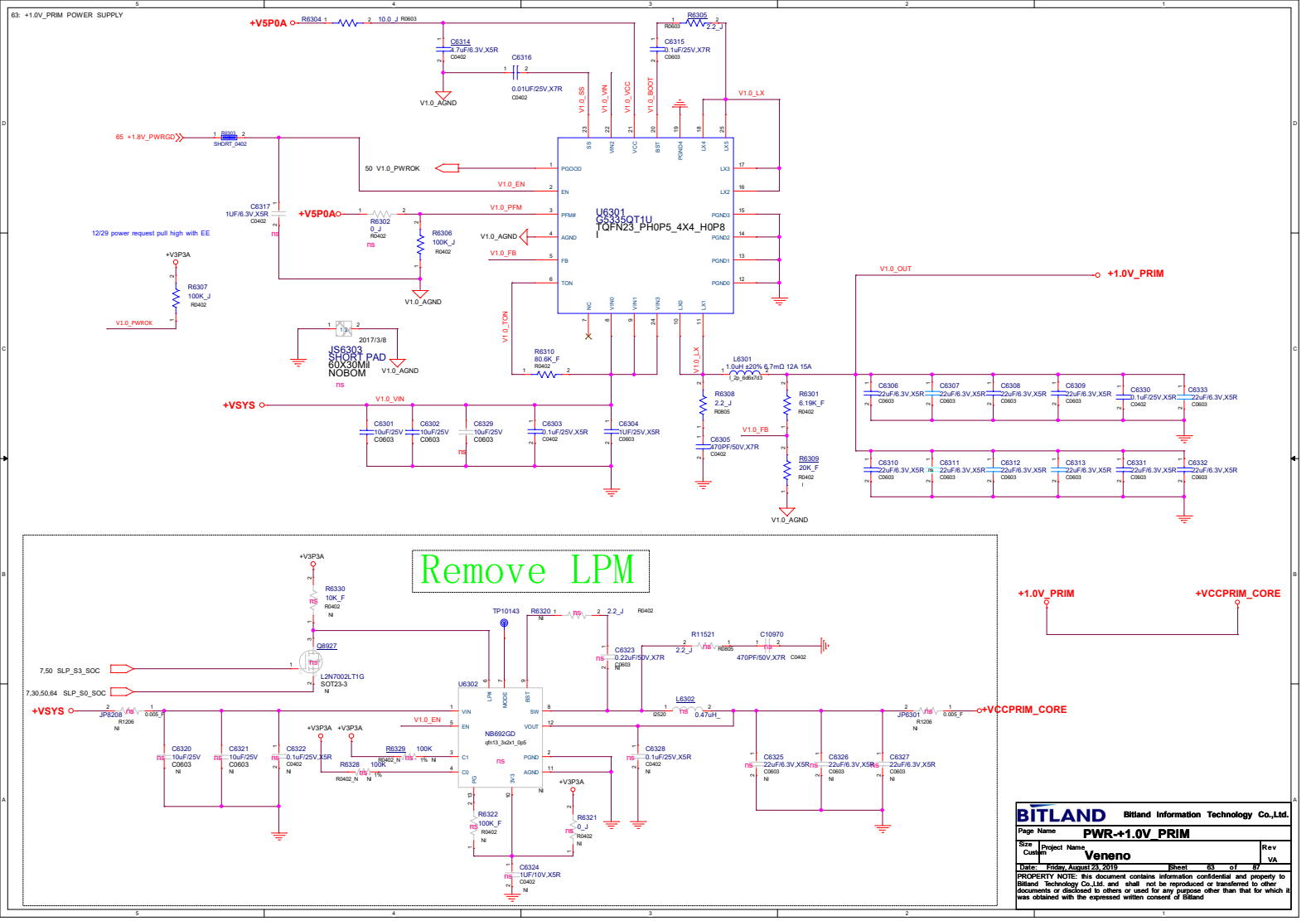

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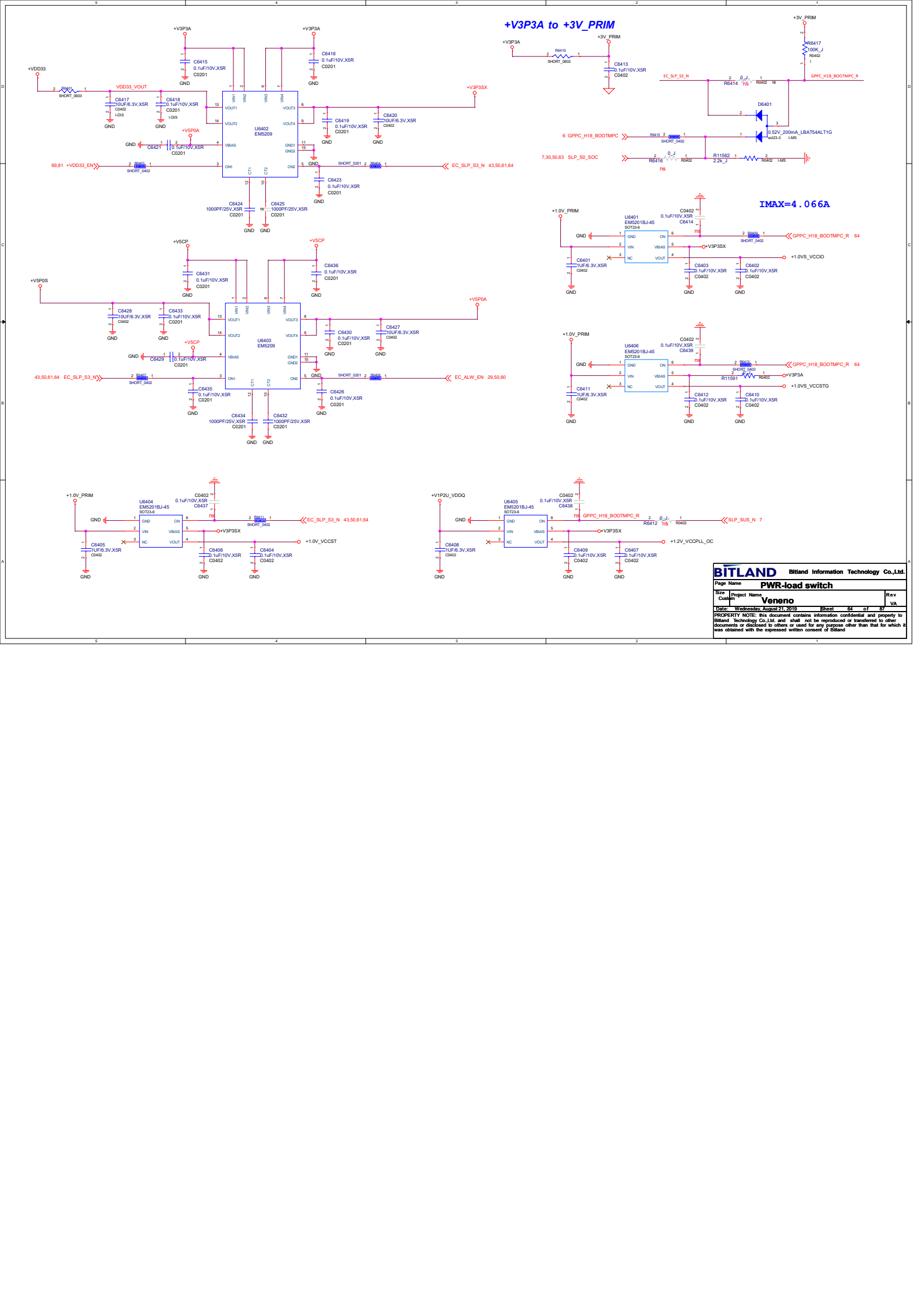
+V3P3A to +3V_PRIM
+V3P3A
+3V_PRIM
R6410
SHORT_0603
C6413
0.1uF/10V_X5R
C0402
R6417
100K_J
R6402
EC_SLP_S3_N
R6414
0_J
GPPC_H18_BOOTMPC_R
D6401
6 GPPC_H18_BOOTMPC
R6415
SHORT_0402
0.52V_200mA_LBAT54ALT1G
sot23-3
7,30,50,63 SLP_S0_SOC
R6416
R11562
2.2k_J
+VDD33
R6401
VDD33_VOUT
C6417
10UF/6.3V_X5R
C6418
0.1uF/10V_X5R
C6415
C6416
U6402
EM5209
+V3P3SX
C6419
C6420
+V5P0A
C6421
C6423
69,81 +VDD33_EN
R6403
EC_SLP_S3_N 43,50,61,64
C6424
1000PF/25V_X5R
C6425
+V5CP
C6431
C6436
+V5P0S
C6428
C6433
U6403
EM5209
C6430
C6427
C6429
43,50,61,64 EC_SLP_S3_N
C6435
C6426
C6434
C6432
EC_ALW_EN 29,50,60
IMAX=4.066A
+1.0V_PRIM
U6401
EM5201BJ-45
SOT23-6
C0402
0.1uF/10V_X5R
C6414
GPPC_H18_BOOTMPC_R 64
+V3P3SX
+1.0VS_VCCIO
C6401
1UF/6.3V_X5R
C6403
C6402
U6406
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C6439
R6413
R11591
+1.0VS_VCCSTG
C6411
C6412
C6410
+1.0V_PRIM
U6404
EM5201BJ-45
C6437
EC_SLP_S3_N 43,50,61,64
+V3P3SX
+1.0V_VCCST
C6405
C6406
C6404
+V1P2U_VDDQ
U6405
EM5201BJ-45
C6438
GPPC_H18_BOOTMPC_R
R6412
SLP_SUS_N 7
+1.2V_VCCPLL_OC
C6408
C6409
C6407
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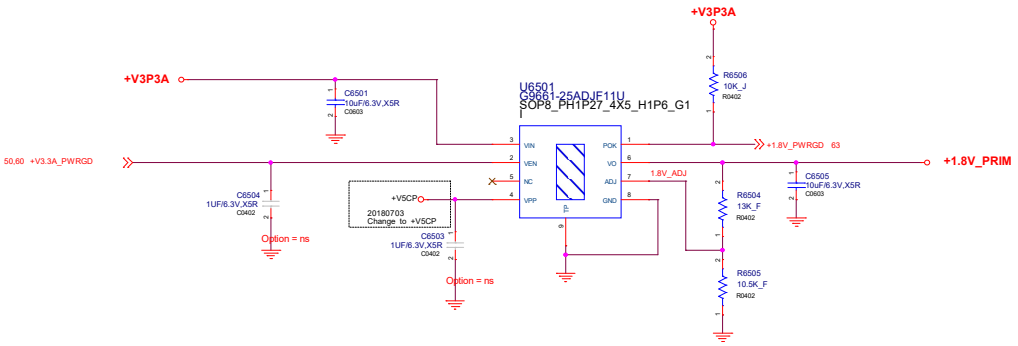

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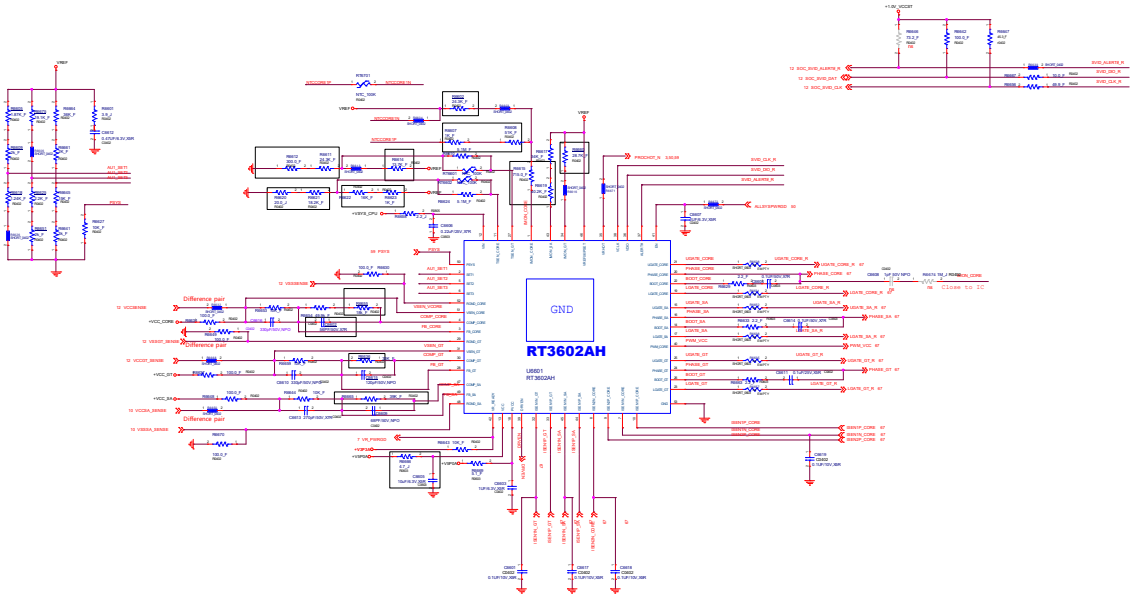

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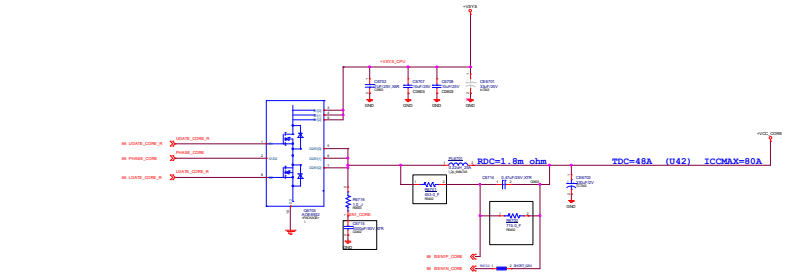

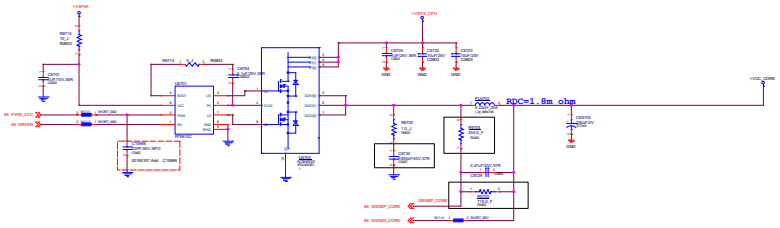

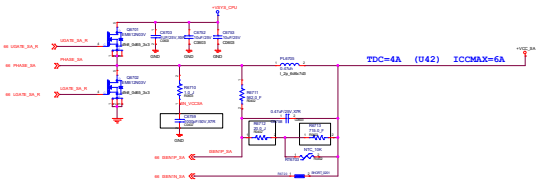

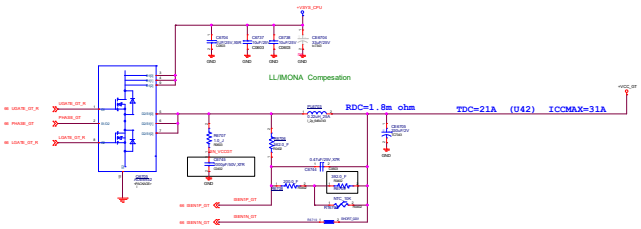

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Page Name: PWR-VCC_CORE/GT/SA

Project Name: Venano

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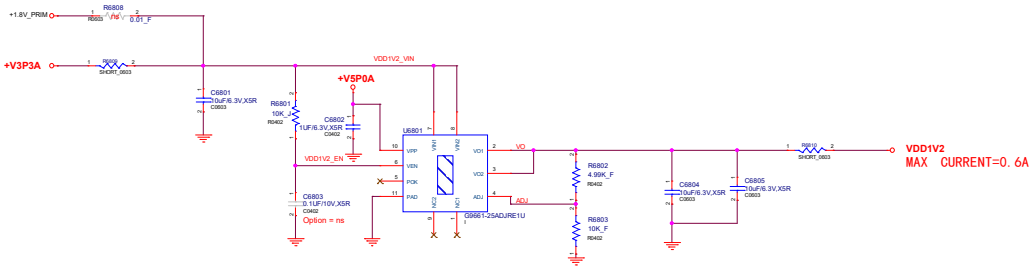

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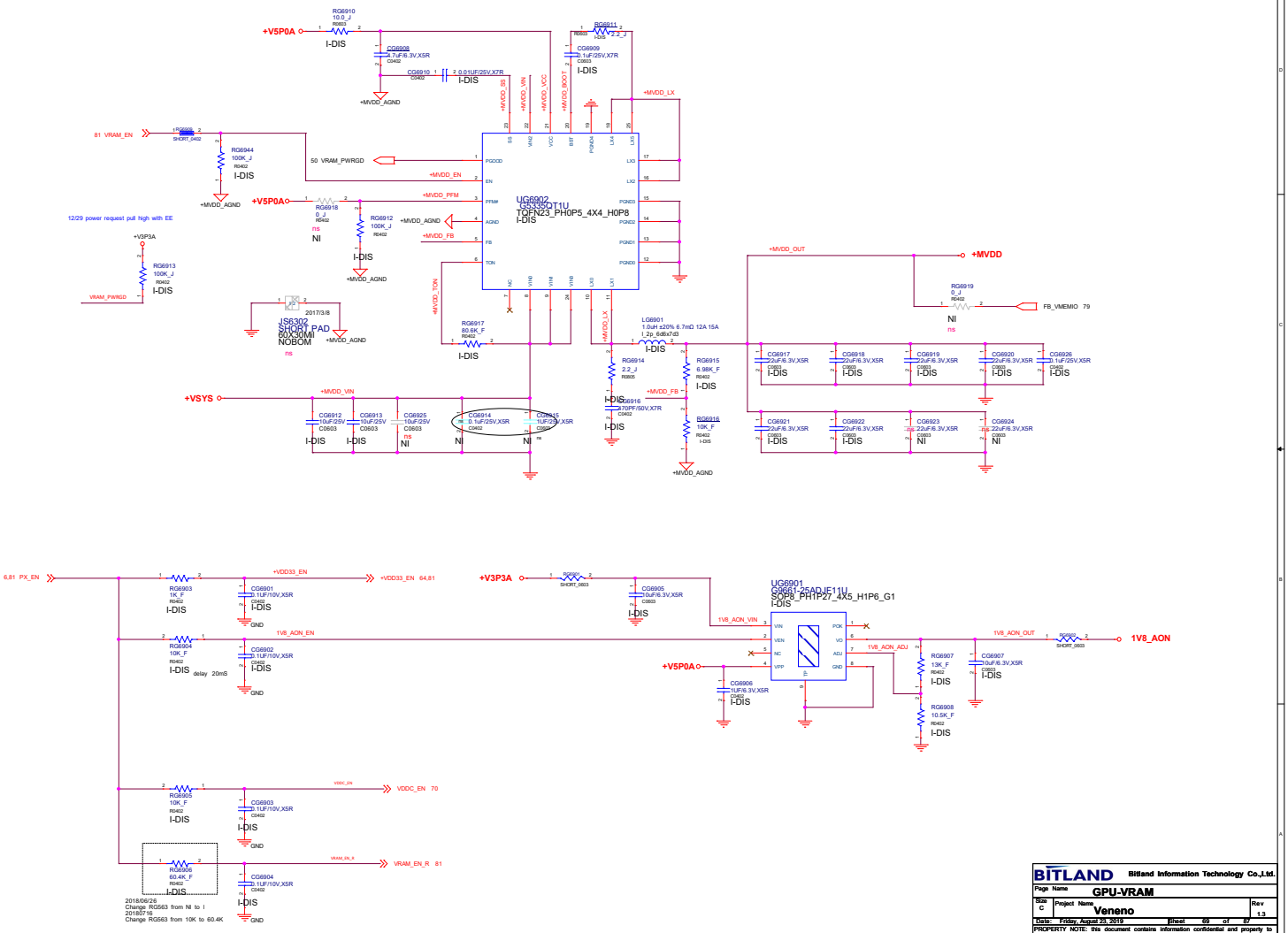

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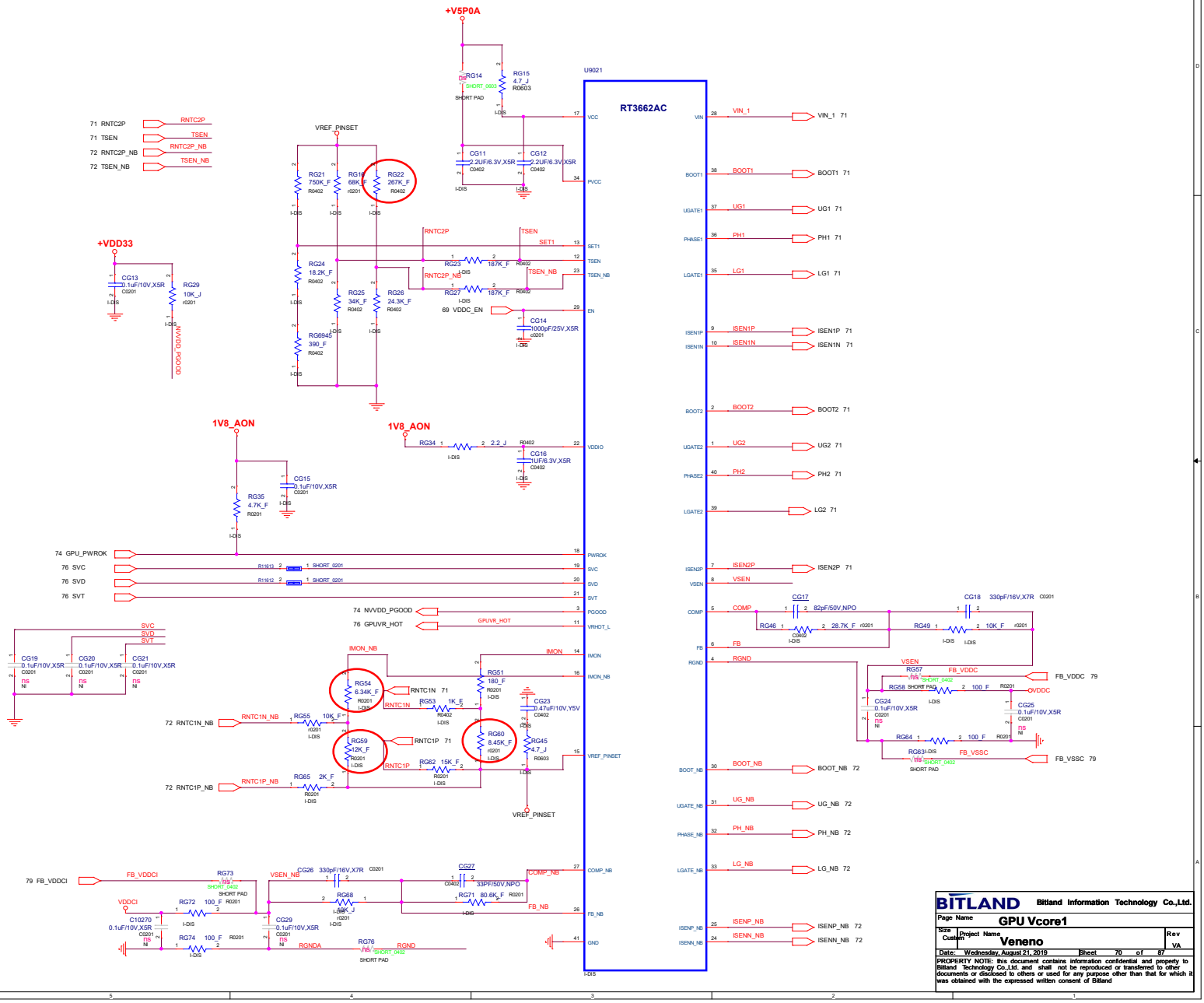
70: GPU POWER



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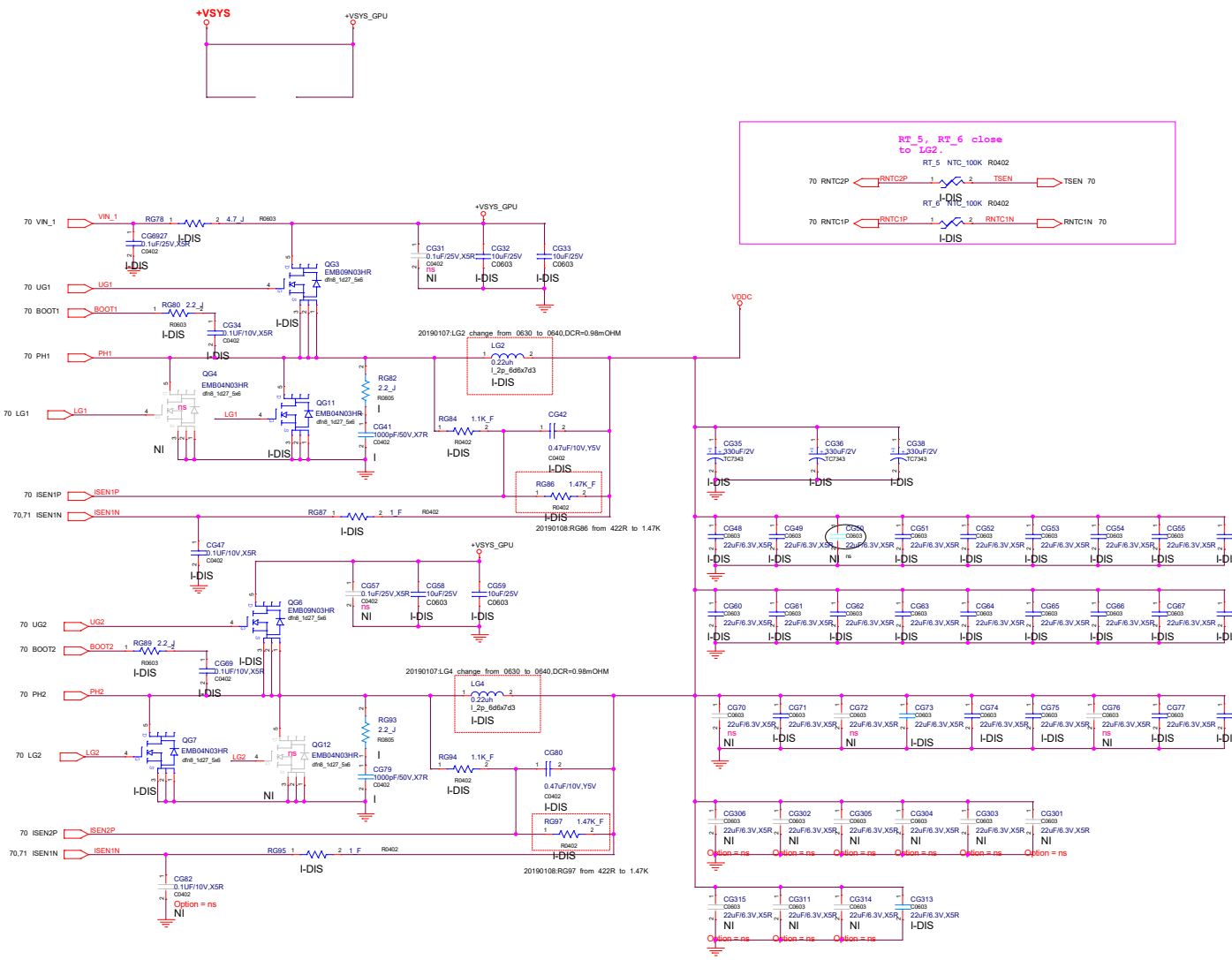

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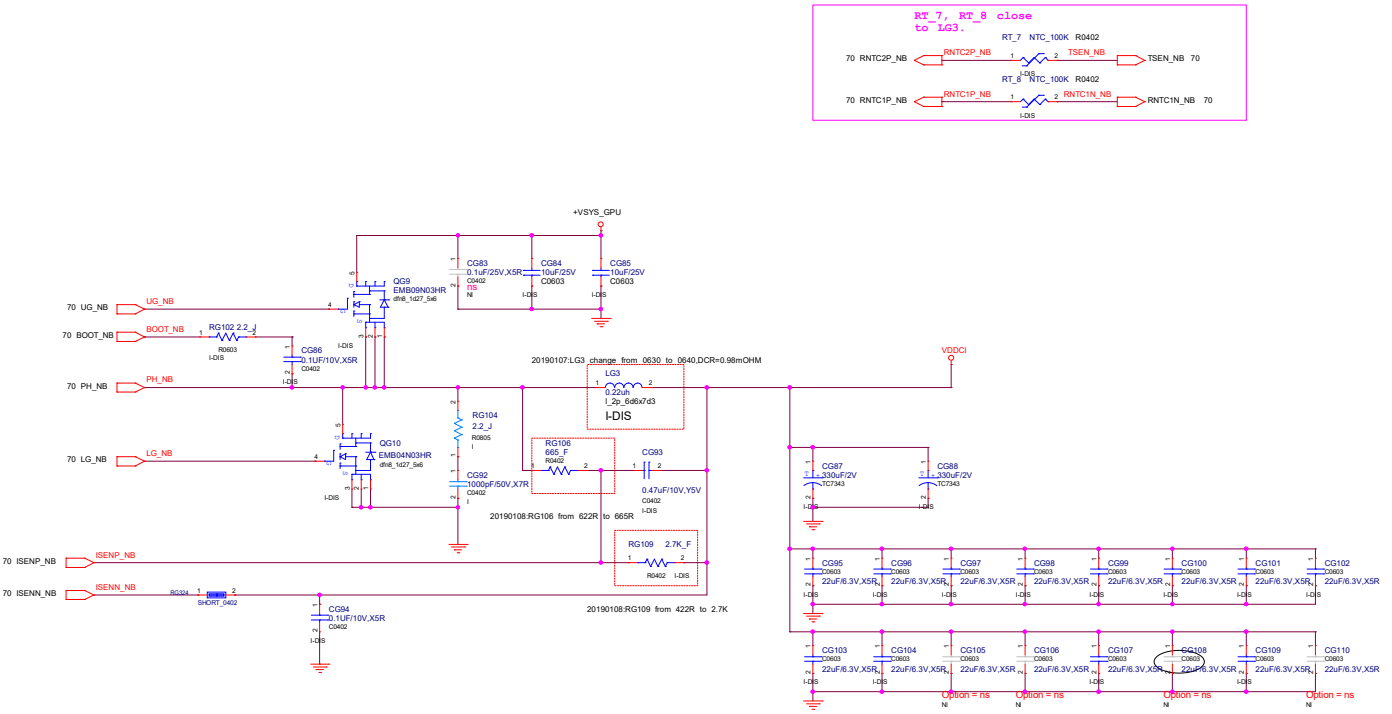

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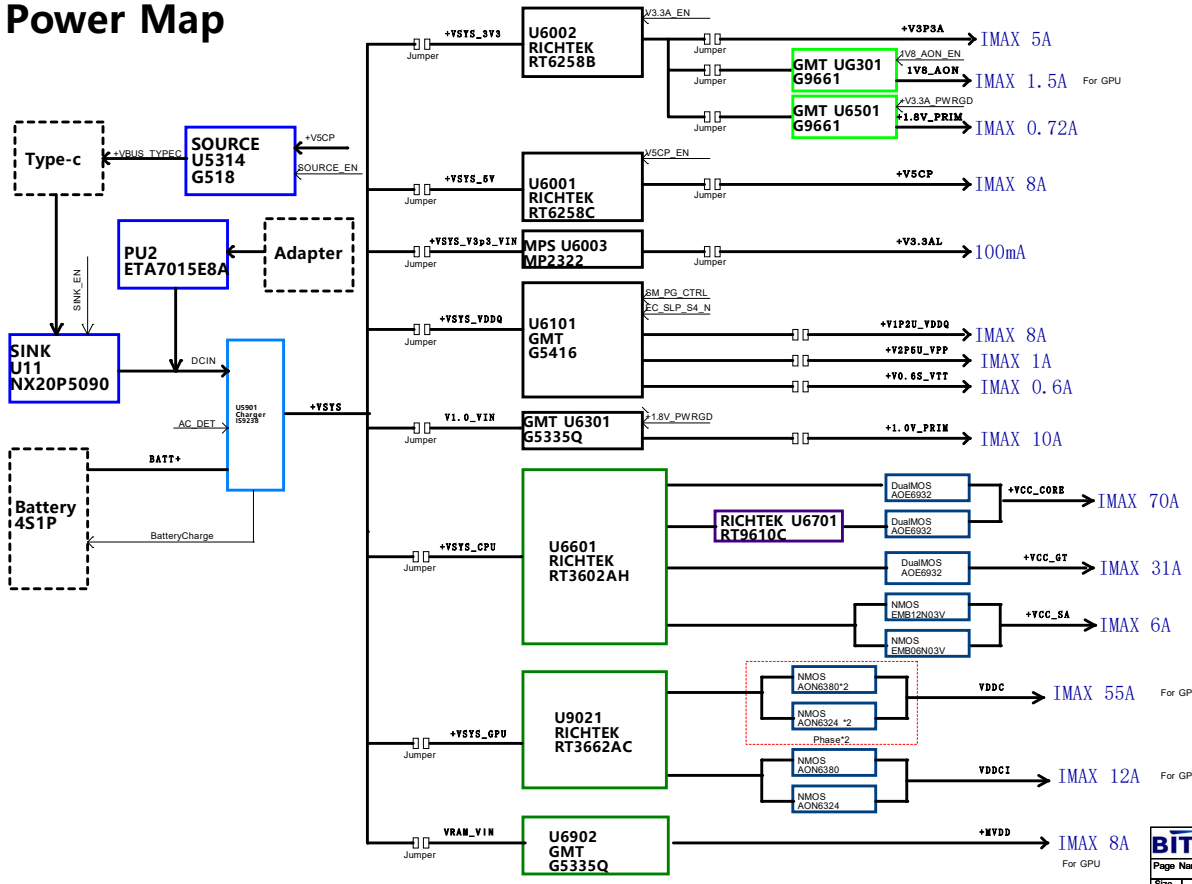
Power Map



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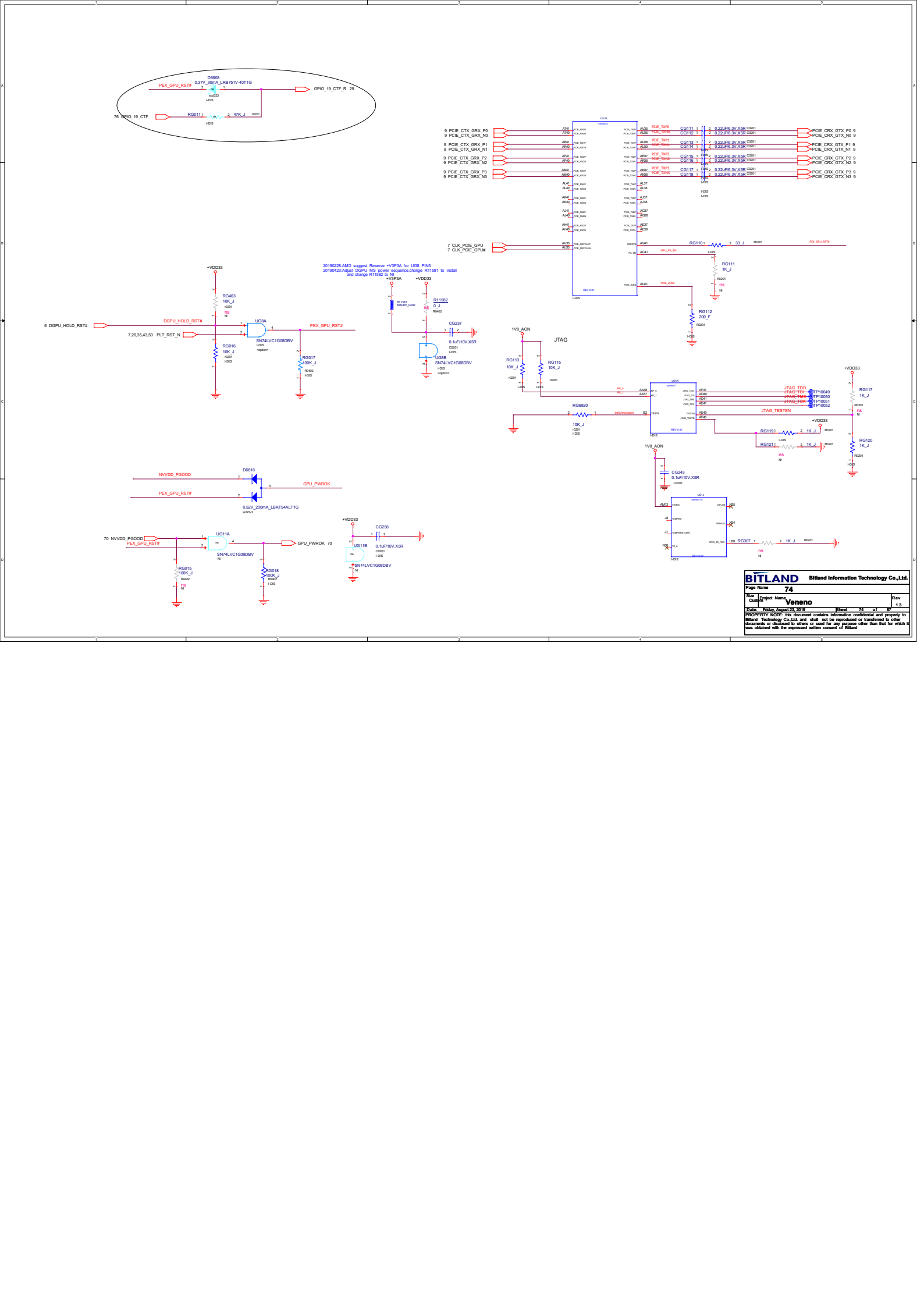

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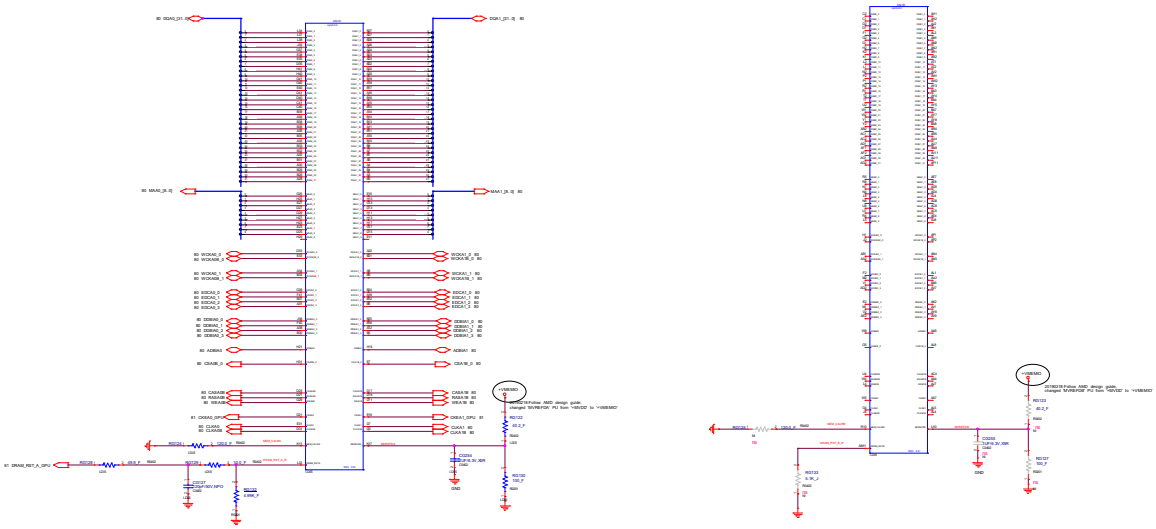

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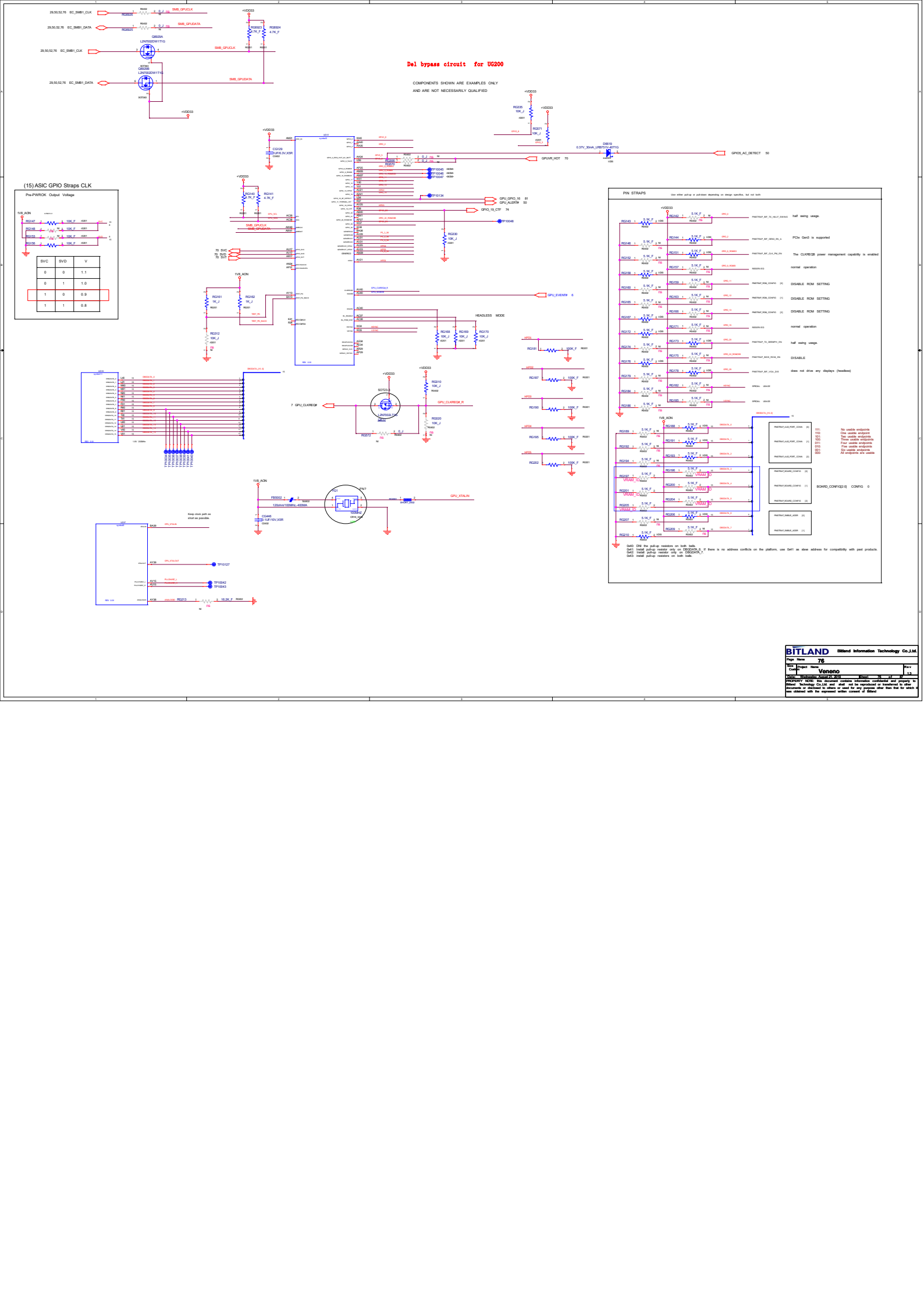
Del bypass circuit for UG200
COMPONENTS SHOWN ARE EXAMPLES ONLY
AND ARE NOT NECESSARILY QUALIFIED
(15) ASIC GPIO Straps CLK
Pre-PWROK Output Voltage
SVC SVD V
0 0 1.1
0 1 1.0
1 0 0.9
1 1 0.8
PIN STRAPS
Use either pull-up or pull-down depending on design specifics, but not both
half swing usage.
PCIe Gen3 is supported
The CLKREQB power management capability is enabled
normal operation
DISABLE ROM SETTING
DISABLE ROM SETTING
DISABLE ROM SETTING
normal operation
half swing usage.
DISABLE
does not drive any displays (headless)
No usable endpoints
One usable endpoint
Two usable endpoints
Three usable endpoints
Four usable endpoints
Five usable endpoints
Six usable endpoints
All endpoints are usable
BOARD_CONFIG[2:0] CONFIG 0
0x40: DNI the pull-up resistors on both balls.
0x41: Install pull-up resistor only on DBIDATA_6. If there is no address conflicts on the platform, use 0x41 as slave address for compatibility with past products.
0x42: Install pull-up resistor only on DBIDATA_7.
0x43: Install pull-up resistors on both balls.
Keep clock path as short as possible.
HEADLESS MODE
GPU_EVENT# 6
GPU_CLKREQ#_R
GPU_XTALIN
GPU_XTALOUT
GPIO5_AC_DETECT 50
GPUVR_HOT 70
GPU_ALERT# 50
GPIO_16_CTF 74
7 GPU_CLKREQ#
SMB_GPUCLK
SMB_GPUDATA
VRAM_ID
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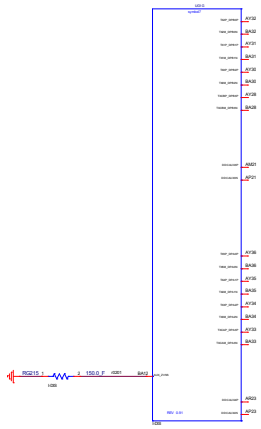
ASIC - TMDP (A/B)



ASIC - TMDP (C/D)

ASIC - TMDP (E)

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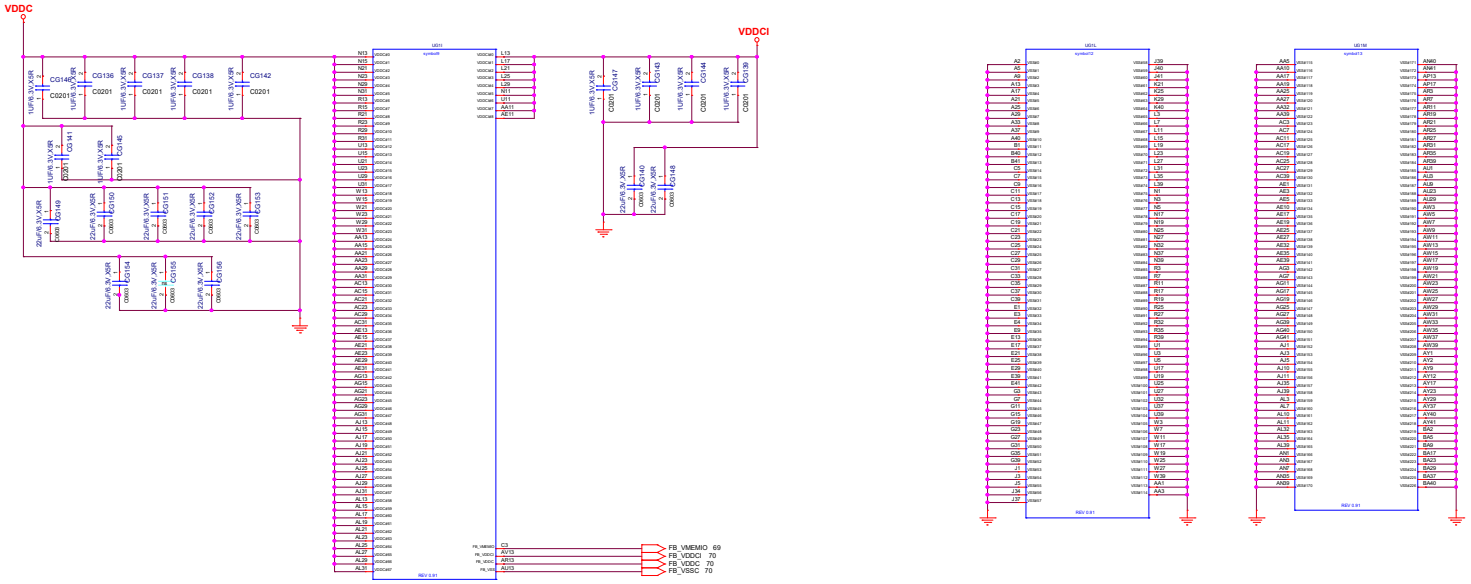

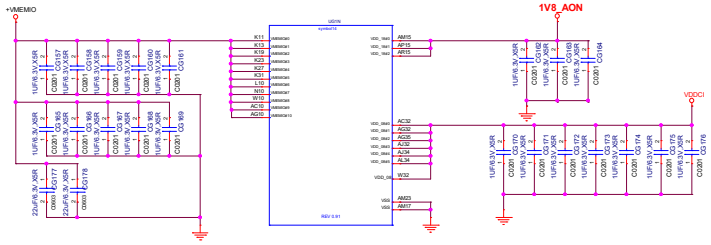

For cost effective designs where VDDCI and VDD_08 are supplied by one regulator, have the VDDCI and VDD_08 balls joined on a unified power plane.

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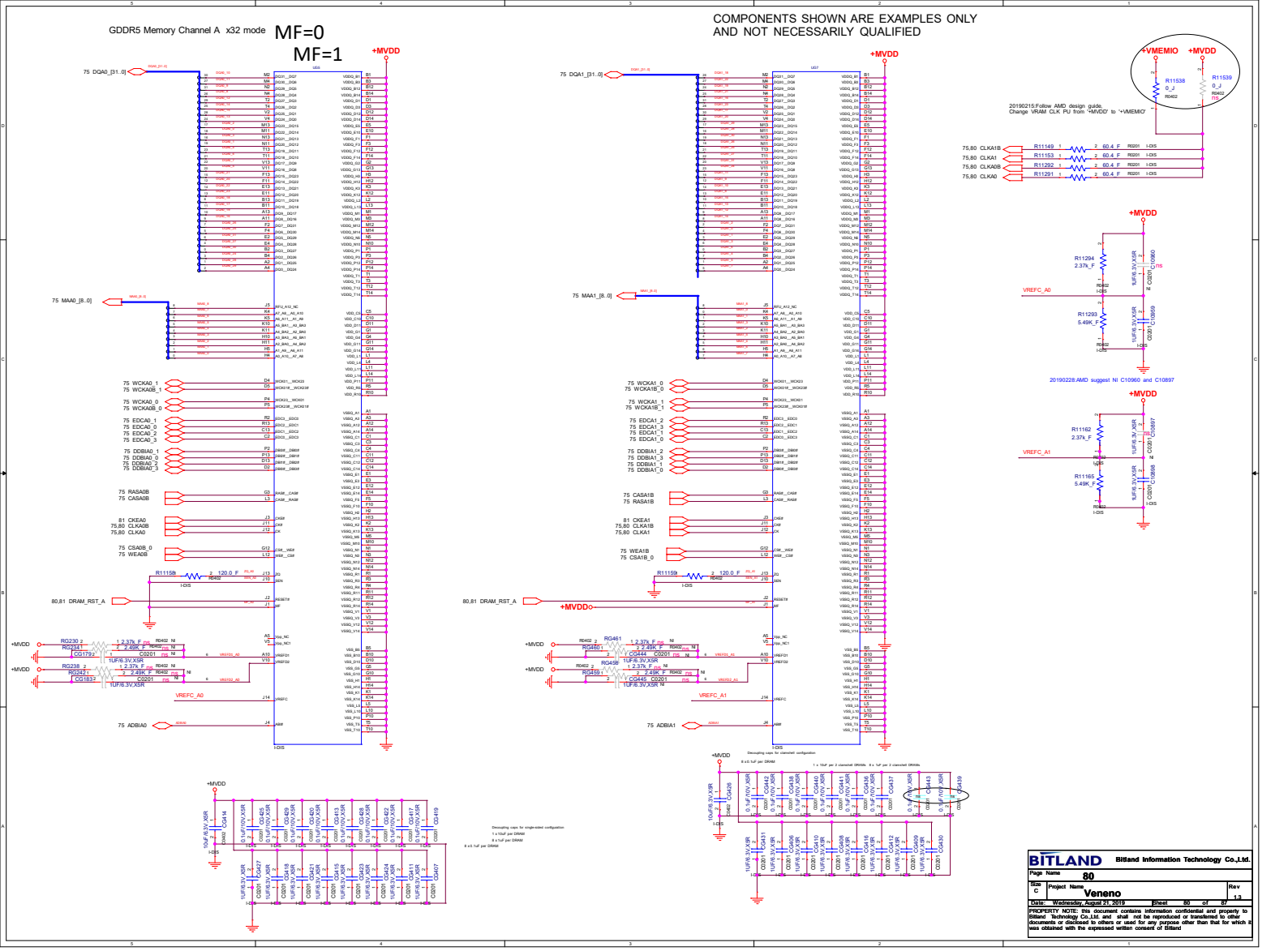
GDDR5 Memory Channel A x32 mode MF=0 MF=1

COMPONENTS SHOWN ARE EXAMPLES ONLY
AND NOT NECESSARILY QUALIFIED



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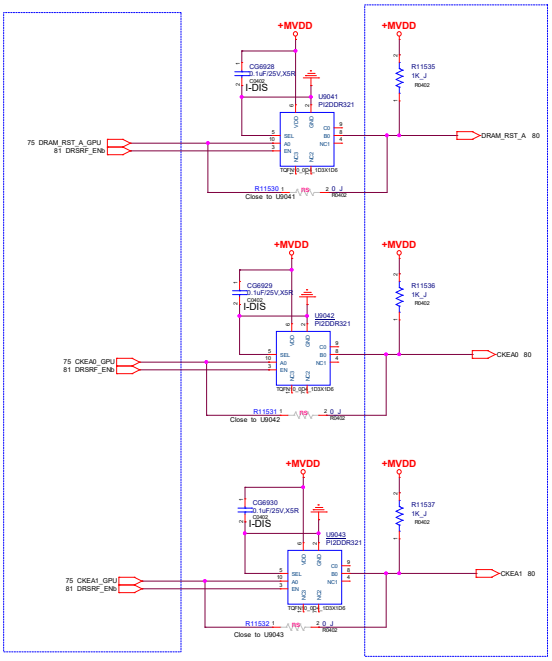

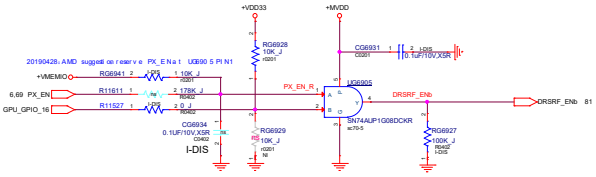

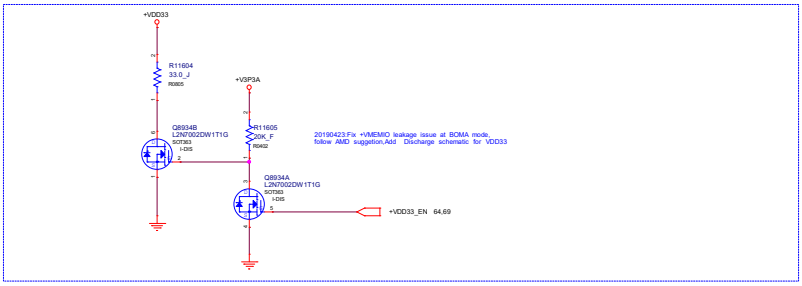

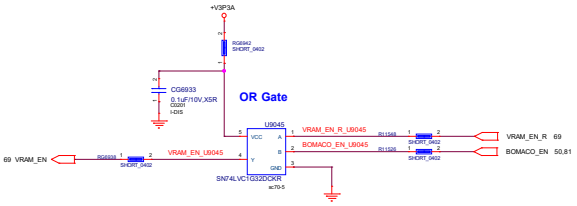

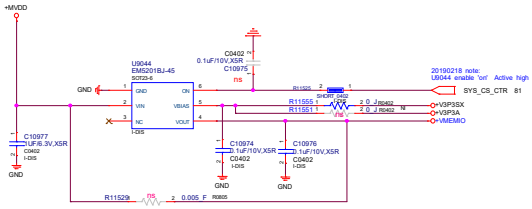

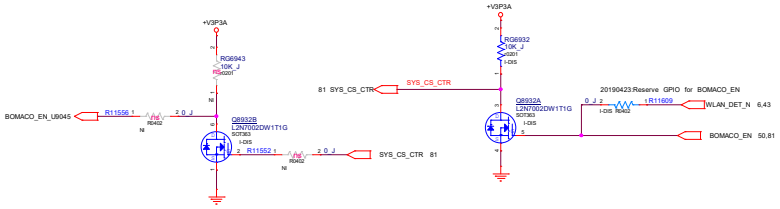

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